ILI6150M6

1536 CH Source Driver with LVDS TCON For 1024RGBx768/600 TFT LCD

Specification
Preliminary

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1. Introduction

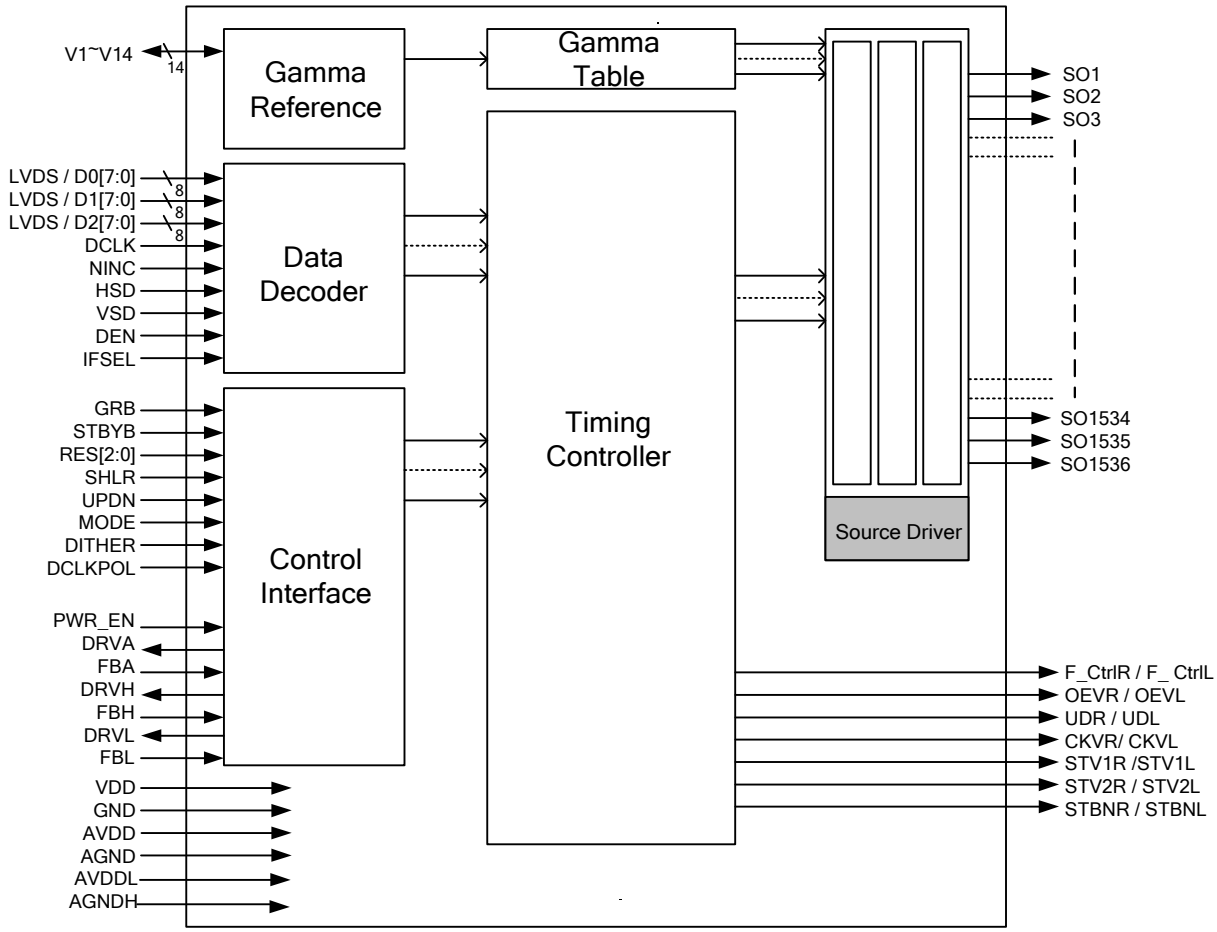
The ILI6150 is a highly integrated solution for small size to middle size a-Si TFT-LCD panels. This chip integrates 1536ch for normal cascade and dual gate mode source driver with LVDS and parallel RGB TTL input interface. This chip is special designed for low cost UMPC application.

2. Features

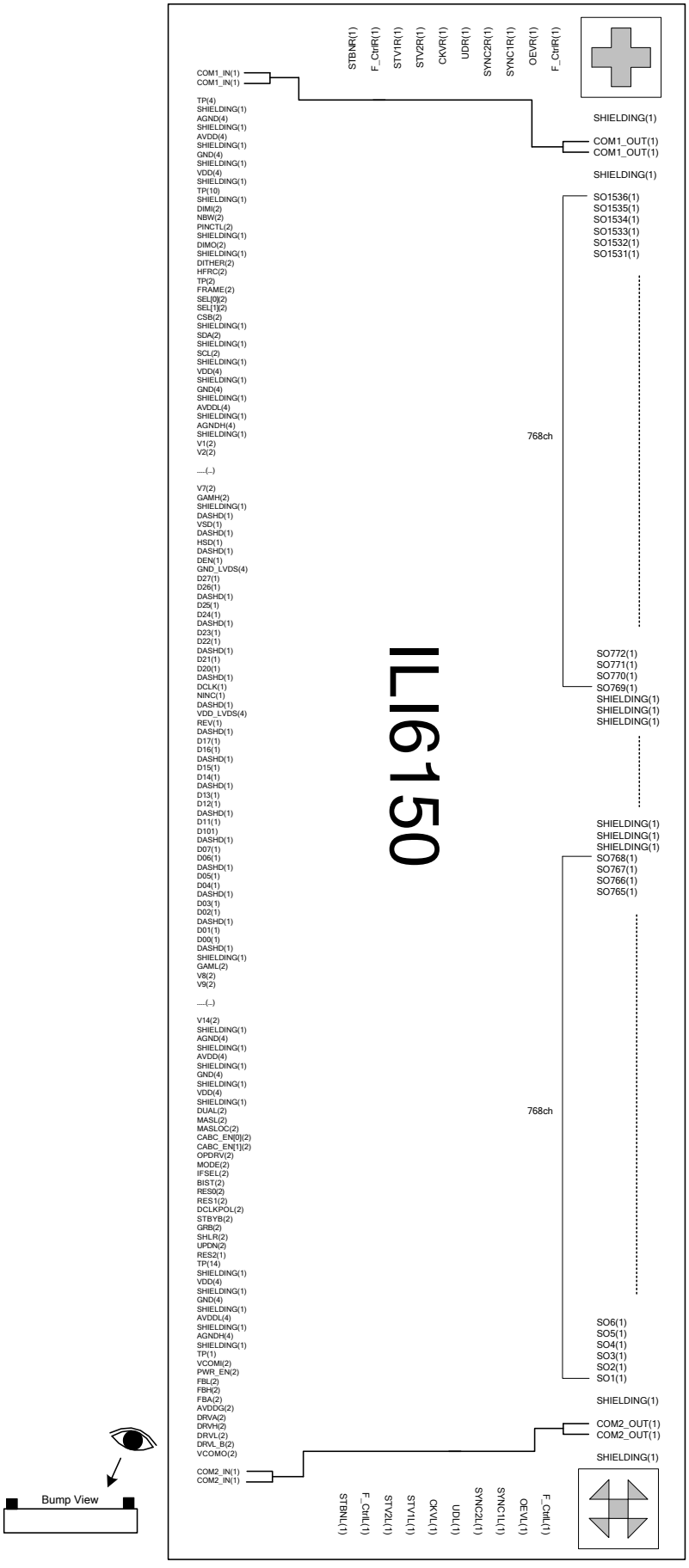
- Special design for 1024RGBX600 TFT LCD Panel with LVDS/TTL 8/8/8 Bits interface
- Integrate 1536 channel source driver with single or dual gate function
- Support cascade function with bidirectional shift control (CMOS signal)
- Support panel resolution (HxV) :

  1024RGBX768, 1024RGBX600, 800RGBX600, 800RGBX480, 960RGBX640, 600RGBX1024
- 8-bit resolution 256 gray-scale with Dithering (6 bits DAC + 2 bit FRC or HFRC)
- Support Pin Control function for Up/Down, Left/Right … control
- Power for digital circuit(VDD): 2.3V ~ 3.6V
- Power for analog circuit(AVDD): 8V ~ 13.5V
- Support Half AVDD voltage for Source Driver Block
- Operating frequency: 71MHz for LVDS interface
- Embedded Gamma Table for special custom request
- V1~V14 for adjusting Gamma correction
- 1 + 2 dot inversion architecture
- Built-In CABC function
- Built-In AUTO BIST pattern
- COG package
- Chip Size : 25000um X 700um、Output bump pitch : 15um

3. Block Diagram

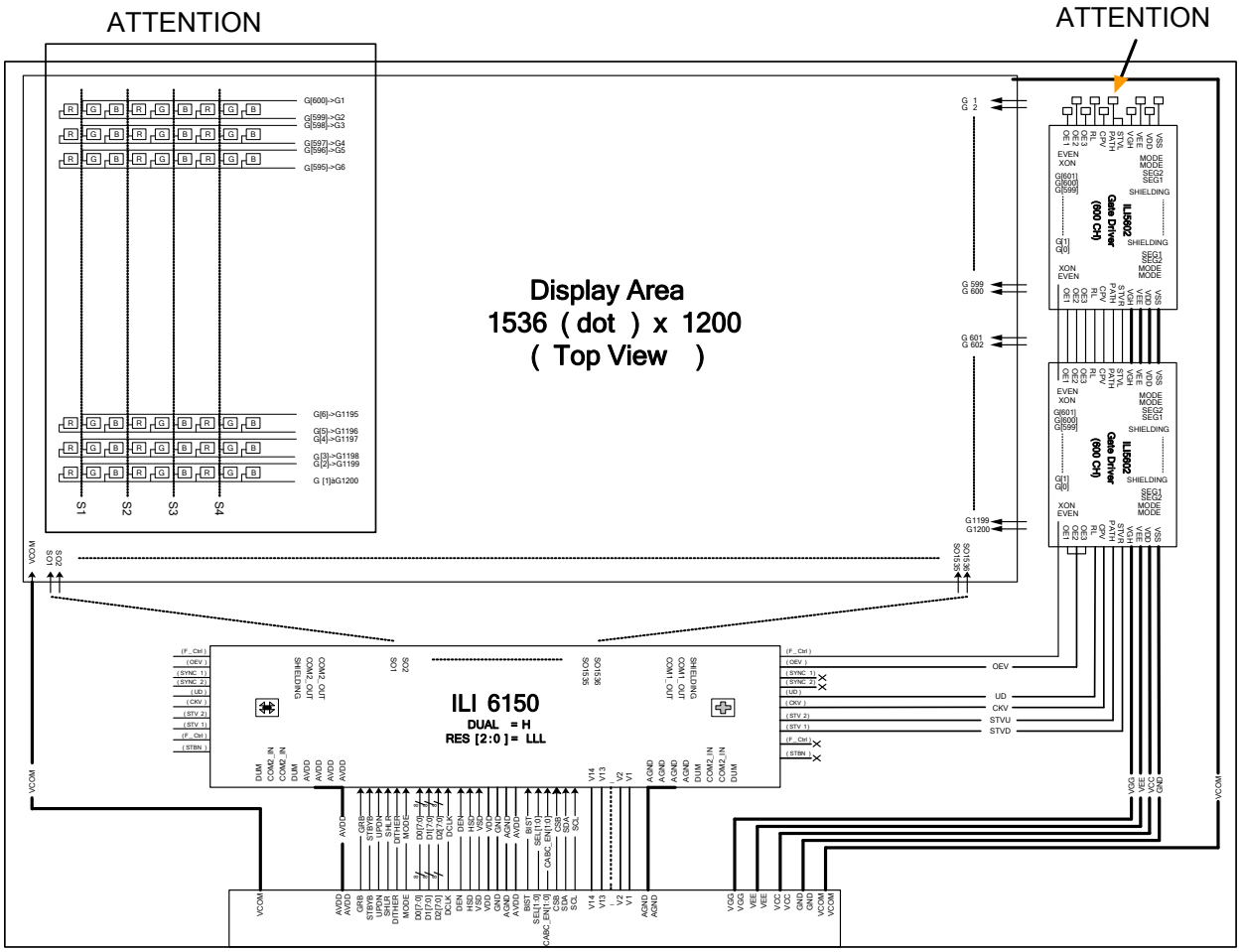


4. Pad Sequence

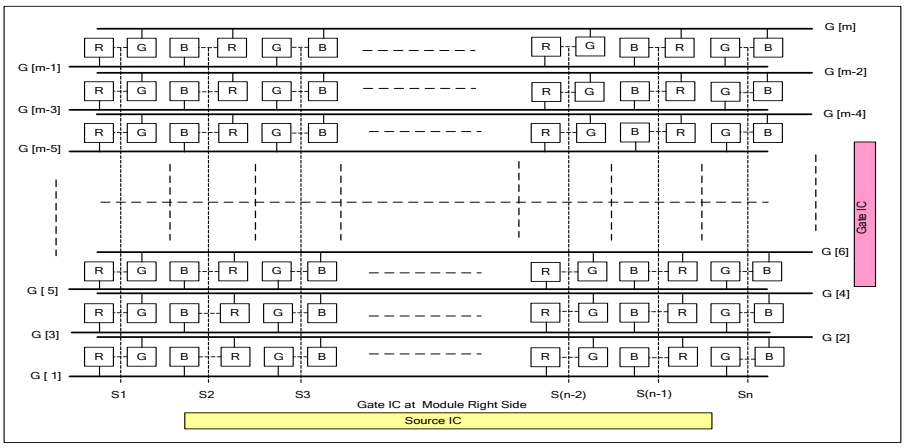


5. Application Block Diagram

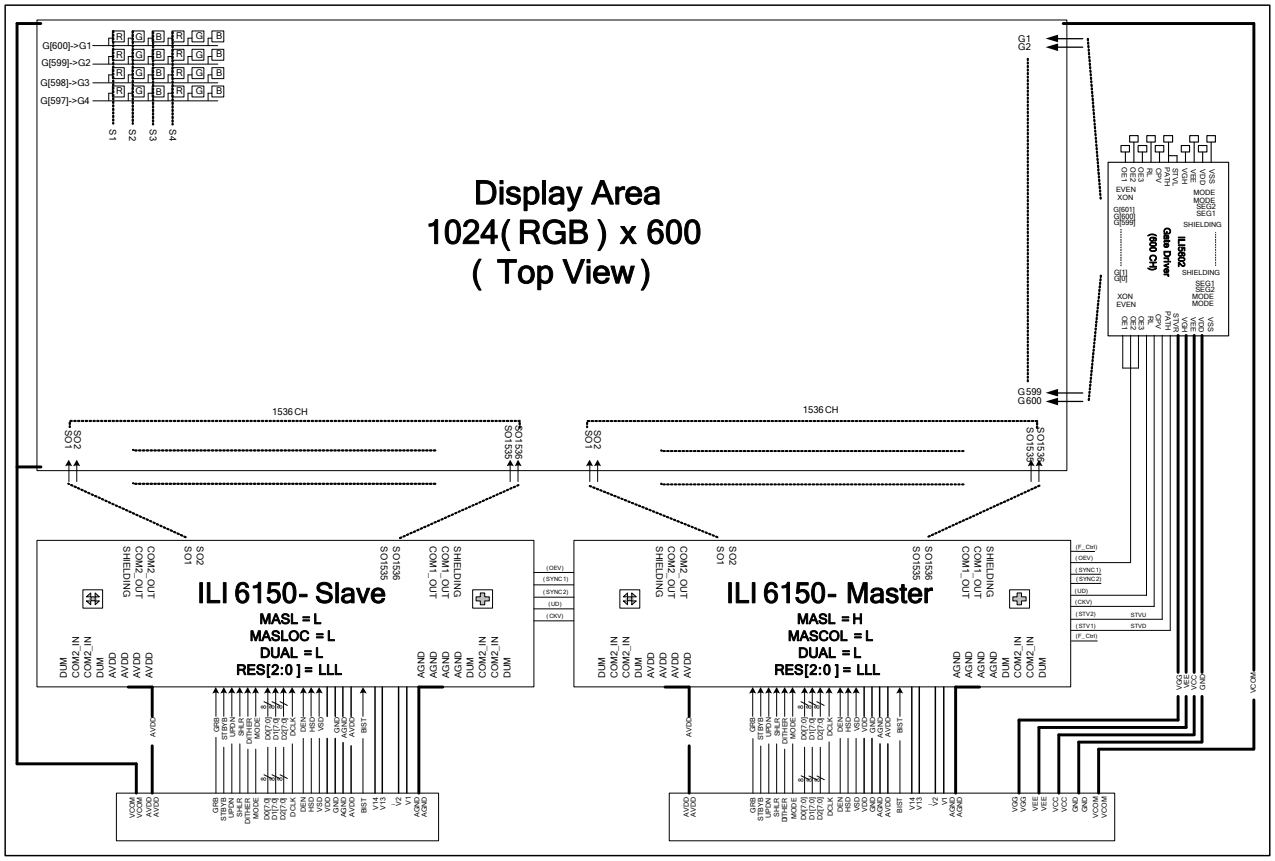
5.1 Dual Gate



5.2 Dual Gate Color Filter Type



5.3 Cascade with Two FPC



6. Pin Descriptions

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>D07 ~ D00
D17 ~ D10
D27 ~ D20</td><td>I</td><td>LVDS or Parallel RGB data Input. Select by “IFSEL” pin.
<table><tr><th>Pin name</th><th>TTL Interface</th><th>LVDS Interface</th></tr><tr><td>IFSEL</td><td>L</td><td>H</td></tr><tr><td>D2[0], D2[1]</td><td>B[0], B[1]</td><td>NIND0, PIND1</td></tr><tr><td>D2[2], D2[3]</td><td>B[2], B[3]</td><td>NIND2, PIND3</td></tr><tr><td>D2[4], D2[5]</td><td>B[4], B[5]</td><td>NIND4, PIND5</td></tr><tr><td>D2[6], D2[7]</td><td>B[6], B[7]</td><td>NIND6, PIND7</td></tr></table>LVDS 6 bit data input : PIND[2:0], NIND[2:0].
D[07:00] = R[7:0] data; D[17:10] = G[7:0] data; D[27:20] = B[7:0] data.
For 18bit RGB interface, connect two LSB bits of all the R/G/B data buses to GND.
Note : D07~D00 SO[1] , SO[4] … SO[1531] , SO[1534]
D17~D10 SO[2] , SO[5] … SO[1532] , SO[1535]
D27~D20 SO[3] , SO[6] … SO[1533] , SO[1536]
Note: Please note the relation between RGB data and Color Filter sequence</td></tr>
<tr><td>DCLK</td><td>I</td><td>Clock Input pin for LVDS or TTL mode. Select by “IFSEL” pin.
<table><tr><th>Pin name</th><th>TTL Interface</th><th>LVDS Interface</th></tr><tr><td>IFSEL</td><td>L</td><td>H</td></tr><tr><td>DCLK</td><td>DCLK</td><td>PINC</td></tr></table></td></tr>
<tr><td>NINC</td><td>I</td><td>Negative LVDS differential clock input.</td></tr>
<tr><td>V1~V14</td><td>I</td><td>Full Range Application:
V1~V14 are the external gamma correction points. The voltage of these pins must be:
AGND+0.1<V14<V13<V12<V11<V10<V9<V8;V7<V6<V5<V4<V3<V2<V1< AVDD-0.1 .

Note:
When used external gamma, GAMH and GAML must tie low</td></tr>
<tr><td>SHLR</td><td>I</td><td>Source Right or Left sequence control. Normally pull high.
SHLR = “L”, shift left: last data = SO[1]←SO[2]←SO[3].....←SO[1536] = first data.
SHLR = “H”, shift right: first data = SO[1]→SO[2]→SO[3].....→SO[1536] = last data.</td></tr>
<tr><td>SEL[1:0]</td><td>I</td><td>Gate on sequence select. Normally pull low
<table><tr><th>SEL[0]</th><th>SEL[1]</th><th>Pin control function</th></tr><tr><td>1</td><td>1</td><td>Z+弓</td></tr><tr><td>1</td><td>0</td><td>弓</td></tr><tr><td>0</td><td>1</td><td>＼ (Inverse Z)</td></tr><tr><td>0</td><td>0</td><td>Z</td></tr></table></td></tr>
<tr><td>CABC_EN[1:0]</td><td>I</td><td>CABC H/W enable pin. Normally pull low
<table><tr><th>CABC_EN1</th><th>CABC_EN0</th><th>Mode</th></tr><tr><td>0</td><td>0</td><td>CABC OFF</td></tr><tr><td>0</td><td>1</td><td>User interface Image</td></tr><tr><td>1</td><td>0</td><td>Still Picture</td></tr><tr><td>1</td><td>1</td><td>Moving Image</td></tr><tr><td colspan="3">Remark: Default CABC OFF</td></tr></table></td></tr>
<tr><td>HSD</td><td>I</td><td><table><tr><th>Pin name</th><th>TTL Interface</th><th>LVDS Interface</th></tr><tr><td>IFSEL</td><td>L</td><td>H</td></tr><tr><td rowspan="2">HSD</td><td rowspan="2">Horizontal Sync input
(Negative polarity)</td><td>L : 8 Bit</td></tr><tr><td>H : 6 Bit</td></tr></table></td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>VSD</td><td>I</td><td>
<table>
<tr><th>Pin name</th><th>TTL Interface</th><th>LVDS Interface</th></tr>
<tr><td>IFSEL</td><td>L</td><td>H</td></tr>
<tr><td>VSD</td><td>Vertical Sync input
(Negative polarity)</td><td>Connected to FPC
and Pull Low</td></tr>
</table>
</td></tr>
<tr><td>DEN</td><td>I</td><td>Data Input Enable. Active High to enable the data input bus under “DE Mode”.
Normally pull low.</td></tr>
<tr><td>MODE</td><td>I</td><td>DE / SYNC mode select under TTL mode. Normally pull high
H: DE mode. L: HSD/VSD mode.</td></tr>
<tr><td>DITHER</td><td>I</td><td>Dithering function enable control. Normally pull low
DITHER = “1”, Enable internal dithering function
DITHER = “0”, Disable internal dithering function</td></tr>
<tr><td>HFRC</td><td>I</td><td>H-FRC selection. Normally pull low
HFRC = H : H-FRC enable
HFRC = L : H-FRC disable
If DITHER = “0” , disable dithering function(H-FRC and FRC disable)</td></tr>
<tr><td>PINCTL</td><td>I</td><td>Enable pin control function. Normally pull high
PINCTL=”0”, Disable pin control function.
PINCTL=”1”, Enable pin control function.
NOTE: The related 3-wire control register bit control will be disabled under INCTL=”1”.</td></tr>
<tr><td>REV</td><td>I</td><td>Controls whether the data of D00~D27 are inverted or not. Normally pulled low.
When “REV”=1 these data will be inverted. EX. “00” → “ 3F”, “07”→ “ 38”, “15”→ “2A”, and so on.</td></tr>
<tr><td>DCLKPOL</td><td>I</td><td>Input clock edge selection. Normally pull low
CLKPOL = “1”, Latch data at DCLK rising edge.
CLKPOL = “0”, Latch data at DCLK falling edge. (Default)</td></tr>
<tr><td>DUAL</td><td>I</td><td>Dual Gate function enables control. Normally pull high
DUAL = “1”, Enable Dual Gate Function. (Default)
DUAL = “0”, Disable Dual Gate Function
Note: Cascade function will be disabled under “dual gate” mode!!</td></tr>
<tr><td>F_CtrlR/F_CtrlL</td><td>O</td><td>Gate driver control signal (For special Gate on sequence).
Note:
In Cascade structure , let this pin floating
In Dual Gate structure, connect this pin to gate driver’s F_Ctrl.
And setting gate driver’s SEL[1:0] to “00” for Z Scan Type.</td></tr>
<tr><td>IFSEL</td><td>I</td><td>TTL and LVDS Interface selection. Normally pull low
IFSEL = L : TTL interface
IFSEL = H : LVDS interface</td></tr>
<tr><td>GAMH</td><td>I</td><td>When INTERNAL Gamma Table is used, GAMH tied to AVDD.
(When used external gamma, GAMH must tie low)</td></tr>
<tr><td>GAML</td><td>I</td><td>When using INTERNAL Gamma Table, tied to GND.
(When used external gamma , GAML must tie low)</td></tr>
<tr><td>GRB</td><td>I</td><td>Global reset pin. Active Low to enter Reset State. Normally pull high.
Suggest to connecting with an RC reset circuit for stability.</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>STBYB</td><td>I</td><td>Standby mode & Normally pulled high.
STBYB = “1”, normal operation
STBYB = “0”, timing controller, source driver will turn off, all output are High-Z</td></tr>
<tr><td>MASL</td><td>I</td><td>Master and Slave Mode selection. Normally pull high.
MASL =”H”, for Master mode. (Default Mode)
MASL =”L”, for Slave mode.
Only the Master chip will issue the Gate and Cascade control signal.</td></tr>
<tr><td>MASLOC</td><td>I</td><td>Master location definition pin. Normally pull low.
MASLOC =”L”, Master locate on right side (Panel top view). (Default Mode)
MASLOC =”H”, Master locate on left side (Panel top view).</td></tr>
<tr><td>RES[2:0]</td><td>I</td><td>Display resolution selection. RES[2:0] Normally pull low
<table>
<tr><th>RES[2:0]</th><th>Resolution</th><th>Enable Channel</th><th>Disable Channel</th></tr>
<tr><td>L L L</td><td>1024X600</td><td rowspan="2">SO[1]~SO[1536]</td><td rowspan="2">--</td></tr>
<tr><td>L L H</td><td>1024X768</td></tr>
<tr><td>L H L</td><td>800X600</td><td rowspan="2">SO[1]~SO[600] ;
SO[937]~SO[1536]</td><td rowspan="2">SO[601]~SO[936]
(Hi-Z)</td></tr>
<tr><td>L H H</td><td>800X480</td></tr>
<tr><td>H L L</td><td>960RGBX540</td><td rowspan="2">SO[1]~SO[720] ;
SO[817]~SO[1536]</td><td rowspan="2">SO[721]~SO[816]
(Hi-Z)</td></tr>
<tr><td>H L H</td><td>960RGBX640</td></tr>
<tr><td>H H L</td><td>600RGBX1024</td><td>SO[1]~SO[450] ;
SO[1087]~SO[1536]</td><td>SO[451]~SO[1086]
(Hi-Z)</td></tr>
<tr><td>H H H</td><td colspan="3">N.A</td></tr>
</table></td></tr>
<tr><td>UPDN</td><td>I</td><td>Gate Up or Down scan control. Normally pull low.
UPDN = “L”, STV2 output vertical start pulse and UD pin output logical “0” to Gate driver.
UPDN = “H”, STV1 output vertical start pulse and UD pin output logical “1” to Gate driver.</td></tr>
<tr><td>BIST</td><td>I</td><td>Normal Operation/BIST pattern select. Normally pull low
BIST = H : BIST(DCLK input is not needed)
BIST = L : Normal Operation</td></tr>
<tr><td>NBW</td><td>T</td><td>Test pin for ILITEK only. Float this pin for normal operation.</td></tr>
<tr><td>FRAME</td><td>I</td><td>Frame inverse or not select. Normally pulled Low
FRAME = “1”, Uniform
FRAME = “0”, Frame inverse (Default)</td></tr>
<tr><td>OEVR/OEVL</td><td>O</td><td>Gate driver control signal (CABC and BIST sync control)</td></tr>
<tr><td>SYNC1R/SYNC1L</td><td>O</td><td>CABC and BIST sync control</td></tr>
<tr><td>SYNC2R/SYNC2L</td><td>O</td><td>CABC and BIST sync control</td></tr>
<tr><td>UDR/UDL</td><td>O</td><td>Gate driver control signal (CABC and BIST sync control)</td></tr>
<tr><td>CKVR/CKVL</td><td>O</td><td>Gate driver control signal (CABC and BIST sync control)</td></tr>
<tr><td>STV1R/STV1L</td><td>O</td><td>Gate driver control signal</td></tr>
<tr><td>STV2R/STV2L</td><td>O</td><td>Gate driver control signal</td></tr>
<tr><td>STBNR/STBNL</td><td>O</td><td>Gate driver control signal</td></tr>
<tr><td>DIMI</td><td>I</td><td>Brightness control signal. Normally pull high</td></tr>
<tr><td>DIMO</td><td>O</td><td>Backlight dimmer signal for external controller.
DIMO = “0”, Turn off external backlight controller
DIMO = “1”, Logical control signal to turn on external backlight controller
NOTE: If CABC OFF, DIMO = DIMI. Else DIMO is controlled by CABC</td></tr>
</table>

Pin Name	I/O	Descriptions
OPDRV	I	Source OP driving selection. **Normally pull low** OPDRV = H : 133% OPDRV = L : normal
CSB	I	Serial communication chip select. **Normally pull High**
SDA	I/O	Serial communication data input. **Normally pull High**
SCL	I	Serial communication clock input. **Normally pull High**
AVDD	PI	Power supply for analog circuits
AGND	PI	Ground pins for analog circuits
VDD	PI	Power supply for digital circuits
GND	PI	Ground pins for digital circuits
VDD_LVDS	PI	LVDS power
GND_LVDS	PI	LVDS ground
AVDDL	PI	Connected to AVDD
AGNDH	PI	Connected to AGND
PWR_EN	I	POWER Enable Function Control Pin. PWR_EN=H, Enable VCOM buffer. PWR_EN=L, Disable VCOM buffer. **Normally pull low.**
FBA	I	N.A (Keep at Open)
DRVA	O	N.A (Keep at Open)
FBH	I	N.A (Keep at Open)
DRVH	O	N.A (Keep at Open)
FBL	I	N.A (Keep at Open)
DRVL	O	N.A (Keep at Open)
DRVL_B	O	N.A (Keep at Open)
VCOMI	I	VCOM buffer in
VCOMO	O	VCOM buffer out
AVDDG	O	N.A (Keep at Open)
SO[1]~SO[1536]	O	Output Driver signal
COM1_IN COM1_OUT	S	Internal link together between input side and output side.
COM2_IN COM2_OUT	S	Internal link together between input side and output side.
VFUSE	T	Test pin for ILITEK only. Float these pins for normal operation.
TPO[1]~TPO[10]	T	Test pin for ILITEK only. Float these pins for normal operation.
TPI[1]~TPI[4]	T	Test pin for ILITEK only. Float these pins for normal operation.

Pin Name	I/O	Descriptions
VREF_PAD	T	Test pin for ILITEK only. Float these pins for normal operation.
SHIELDING	SH	IC Shielding pads. Those pins are internally connected to the AGND. RECOMMAND to add shielding lines on the FPC to reduce EMI.
DASHD	SH	Data Bus Shielding pad. Those pins are internally connected to the GND. RECOMMAND to add shielding lines on the FPC to reduce EMI.
DUM	D	Dummy pads. Those pins are floating pads.

Note:

IO Define	Function
I	Input
O	Output
P	Power
D	Dummy
S	Shorted Line
M	Mark
PI	Power Input
PO	Power Output
T	Testing
SH	Sgielding
I/O	Input/Output
PS	Power Setting

ILI6150 Pass Line Description:

PASS LINE NO.	PAN NAME	
1	COM1_IN	COM1_OUT
2	COM2_IN	COM2_OUT

7. Value of Wiring Resistance

The recommended wiring resistance values are shown below. The wiring resistance values affect the current capacity of the power supply, so be sure to design using values that do not exceed those recommended.

Pin Name	Wiring resistance Value(ohm)	Pin Name	Wiring resistance value(Ω)
AVDD	<5	RES0	<100
AGND	<5	RES1	<100
VDD	<5	RES2	<100
GND	<5	SHLR	<100
V1~V14	<5	UPDN	<100
DRVx	<5	BIST	<100
FBx	<5	MODE	<100
VCOMI	<5	DCLKPOL	<100
VCOMO	<5	DIMO	<100
D00~D07	<5	IFSEL	<100
D10~D17	<5	F_Ctrlx	<500
D20~D27	<5	OEVx	<500
DCLK	<5	UDx	<500
NINC	<5	CKVx	<500
VSD	<20	STV1x	<500
HSD	<20	STV2x	<500
DEN	<20	STBNx	<500
GRB	<100	AVDDL	<5
STBYB	<100	AGNDH	<5
DITHER	<100		

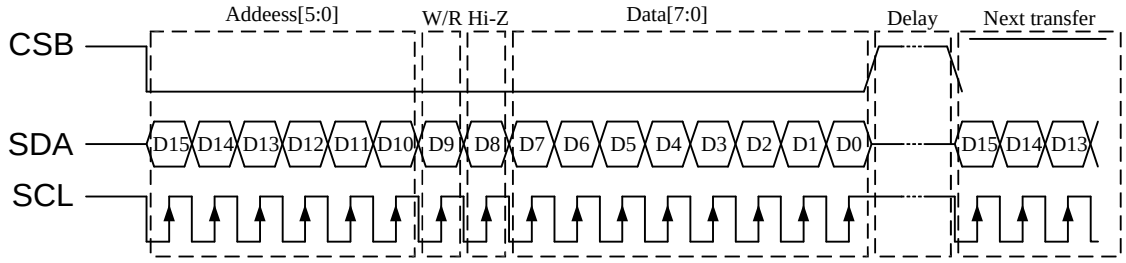
8. 3-Wire Serial Port Interface

8.1 3-Wire Command Format

ILI6150 use the 3-wire serial port as communication interface for all the function and parameter setting.3-Wire Communication can be bi-directional controlled by the "R/W" bit in address field. ILI6150 3-Wire engine act as a "slave mode" for all the time, and will not issue any command to the 3-Wire bus itself.

Under read mode, 3-Wire engine will return the data during "Data phase". The returned data should be latched at the rising edge of SCL by external controller. Data in the "Hi-Z phase" will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under "Hi-Z phase" and "Data phase".

Each Read/Write operation should be exactly 16 bit. To prevent from incorrect setting of the internal register, any write operation with more or less than 16 bit data during a CSB Low period will be ignored by 3-Wire engine. For prevent from incorrect setting of the internal register. Please refer to the section of "3-Wire Timing Diagram" for the detail timing.



3-Wire Command Format:

Bit	Description
D15-D10	Register Address [5:0].
D9	W/R control bit. "0" for Write; "1" for Read
D8	Hi-Z bit during read mode. Any data within this bits will be ignored during write mode
D7-D0	Data for the W/R operation to the address indicated by Address phase

3-Wire Writer Format:

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D1
Register Address[5:0]						0	X	DATA(Issue by external controller)							

3-Wire Read Format:

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D1
Register Address[5:0]						1	Hi-Z	DATA(Issue by 3-Wire engine)							

8.2 3-Wire Control Registers

Following table list all the 3-Wire control registers and bit name definition for ILI6150. Refer to the next section for detail register function description, please.

Setting of all the 3-Wire registers will take effect at the coming falling edge of VSD except GRB and STB bit.

Command Function	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
	Address						R/W	X/Hi-Z	Data Bit							
R0 System Control Register	0	0	0	0	0	0	0	X	PWR_EN	--	LR	UD	STB	GRB	CLKPOL	MODE
									0	--	1	0	1	1	0	1
	00H								2DH							
R1 System Control Register	0	0	0	0	0	1	0	X	CABC1	CABC0	HFRC	DIT	BIST	RESL1	RESL0	RESL2
									0	0	0	0	0	0	0	0
	01H								00H							

R0: System Control Register

Designation	Data Bit	Description
MODE	R0[0]	DE / SYNC mode select. MODE="0", HSD/VSD mode. **MODE="1", DE mode. (Default)**
DCLKPOL	R0[1]	DCLK polarity control bit. **DCLKPOL="0": Data sampling at DCLK falling edge. (Default)** DCLKPOL="1": Data sampling at DCLK rising edge.
GRB	R0[2]	Global reset bit. GRB="0", The controller is in reset state. **GRB="1", Normal operation. (Default)**
STBYB	R0[3]	Standby mode selection bit. STBYB="0", Timing control, driver and DC-DC converter, are off, and all outputs are High-Z. **STBYB="1", Normal operation. (Default)**
UPDN	R0[4]	G Gate Up or Down scan control. **UPDN = "0", STV2 output vertical start pulse and UD pin output logical "0" to Gate driver. (Default)** UPDN = "1", STV1 output vertical start pulse and UD pin output logical "1" to Gate driver
SHLR	R0[5]	Right/Left sequence control of source drive SHLR="0", Shift left: Last data=SO[1]<-SO[2]<-SO[3] … <-SO[1536]=First data. **SHLR="1", Shift right: First data=SO[1]->SO[2]->SO[3] … ->SO[1536]=Last data. (Default)**
	R0[6]	Reserved
PWR_EN	R0[7]	POWER Enable Function Control Pin. PWR_EN=H, Enable PWM & Charge Pump Circuit. PWR_EN=L, Disable PWM & Charge Pump Circuit. **Normally pull low.**

R1: System Control Register

Designation	Address	Description
RES[2:0]	R1[2:0]	Display resolution selection.

RES[2:0]	Resolution	Enable Channel	Disable Channel
L L L	1024X600	SO[1]~SO[1536]	--
L L H	1024X768		
L H L	800X600	SO[1]~SO[600] ; SO[937]~SO[1536]	SO[601]~SO[936] (Hi-Z)
L H H	800X480		
H L L	960RGBX540	SO[1]~SO[720] ; SO[817]~SO[1536]	SO[721]~SO[816] (Hi-Z)
H L H	960RGBX640		
H H L	600RGBX1024	SO[1]~SO[450] ; SO[1087]~SO[1536]	SO[451]~SO[1086] (Hi-Z)

<table>
<tr><td></td><td></td><td><table><tr><td>H H H</td><td>N.A</td></tr></table></td></tr>
<tr><td>BIST</td><td>R1[3]</td><td>Normal Operation/BIST pattern select.
BIST = H : BIST(DCLK input is not needed)
BIST = L : Normal Operation (Default)</td></tr>
<tr><td>DITHER</td><td>R1[4]</td><td>Dithering function enable control.
DITHER = “1”, Enable internal dithering function
DITHER = “0”, Disable internal dithering function (Default)</td></tr>
<tr><td>HFRC</td><td>R1[5]</td><td>H-FRC selection.
HFRC = H : H-FRC enable
HFRC = L : H-FRC disable (Default)
If DITHER = “0” , disable dithering function(H-FRC and FRC disable)</td></tr>
<tr><td>CABC_EN[1:0]</td><td>R1[7:6]</td><td>CABC H/W enable pin. Normally pull low.
<table>
<tr><th>CABC_EN1</th><th>CABC_EN0</th><th>Mode</th></tr>
<tr><td>0</td><td>0</td><td>CABC OFF</td></tr>
<tr><td>0</td><td>1</td><td>User interface Image</td></tr>
<tr><td>1</td><td>0</td><td>Still Picture</td></tr>
<tr><td>1</td><td>1</td><td>Moving Image</td></tr>
<tr><td colspan="3">Remark: Default CABC OFF</td></tr>
</table></td></tr>
</table>

9. Function Description

9.1 Power On/Off Sequence

To prevent the device damage from latch up, the power On-Off sequence must be followed.

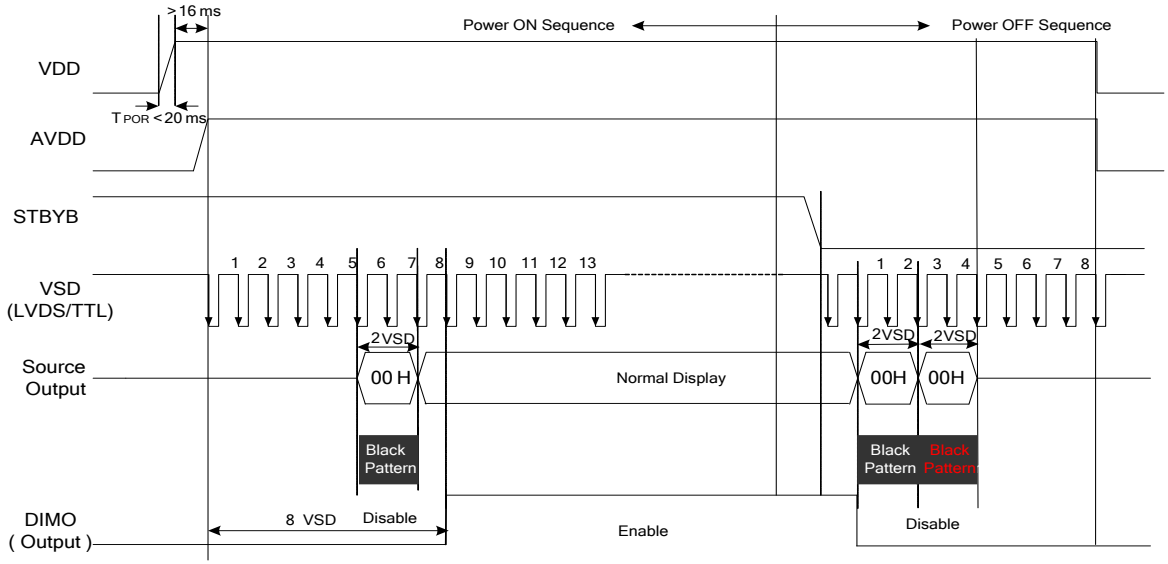
Power On: VDD,GND→AVDD(AVDDL),AGND(AGNDH)→V1~V14→Input Signals

Power Off: Input Signals→V1~V14→ AVDD(AVDDL),AGND(AGNDH)→ VDD,GND

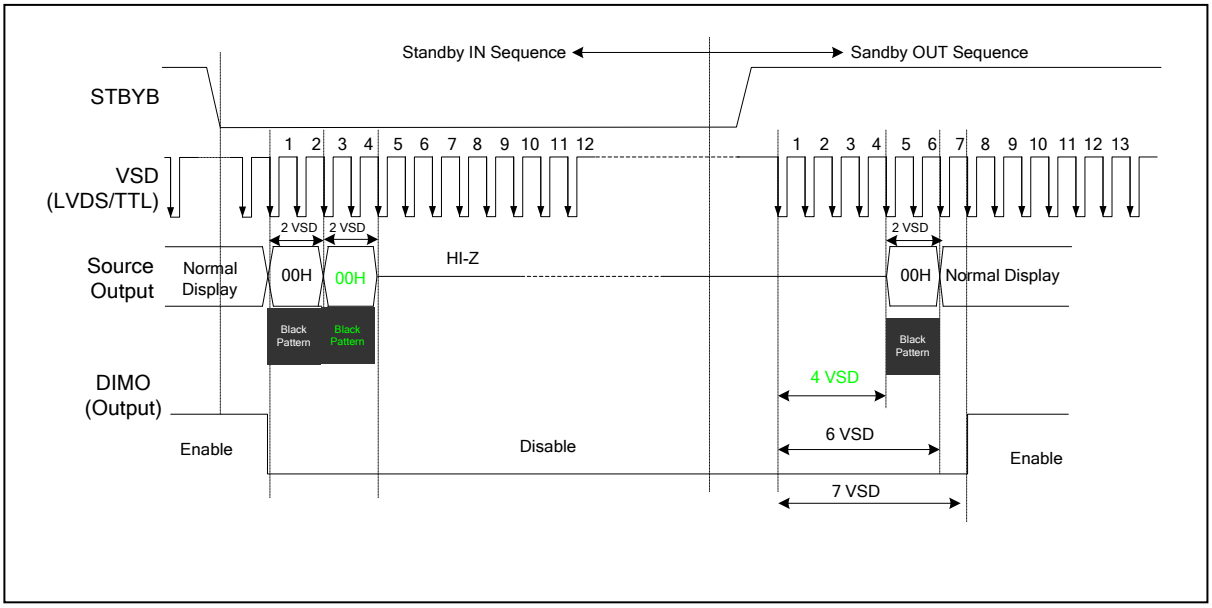
9.2 Power On/Off and Standby Control

In order to prevent IC from power on reset fail, the rising time (T_{POR}) of the digital power supply VDD should be maintained within the given specifications. Refer to “AC Characteristics” for more detail on timing.

9.3 Power On-Off Sequence Timing



9.4 Standby On-Off Sequence Timing



9.5 Input Data VS Output Channels

1. DUAL= 0

(1) SHLR = 1, right shift

Output	SO[1]	SO[2]	SO[3]	---	SO[1534]	SO[1535]	SO[1536]
Order	First data			→	Last data		
Odd Line	D07~D00	D17~D10	D27~D20	---	D07~D00	D17~D10	D27~D20
Evne Line	D07~D00	D17~D10	D27~D20	---	D07~D00	D17~D10	D27~D20

(2) SHLR = 0, left shift

Output	SO[1]	SO[2]	SO[3]	---	SO[1534]	SO[1535]	SO[1536]
Order	First data			←	Last data		
OddLine	D07~D00	D17~D10	D27~D20	---	D07~D00	D17~D10	D27~D20
Evne Line	D07~D00	D17~D10	D27~D20	---	D07~D00	D17~D10	D27~D20

2. DUAL= 1

(1) SHLR = 1, right shift

Output	SO[1]	SO[2]	SO[3]	---	SO[1534]	SO[1535]	SO[1536]
Order	First data			→	Last data		
Odd Line /Gn	D07~D00	D27~D20	D17~D10	---	D07~D00	D27~D20	D17~D10
Odd Line /Gn+1	D17~D10	D07~D00	D27~D20	---	D17~D10	D07~D00	D27~D20
Evne Line Gn	D07~D00	D27~D20	D17~D10	---	D07~D00	D27~D20	D17~D10
Evne Line Gn+1	D17~D10	D07~D00	D27~D20	---	D17~D10	D07~D00	D27~D20

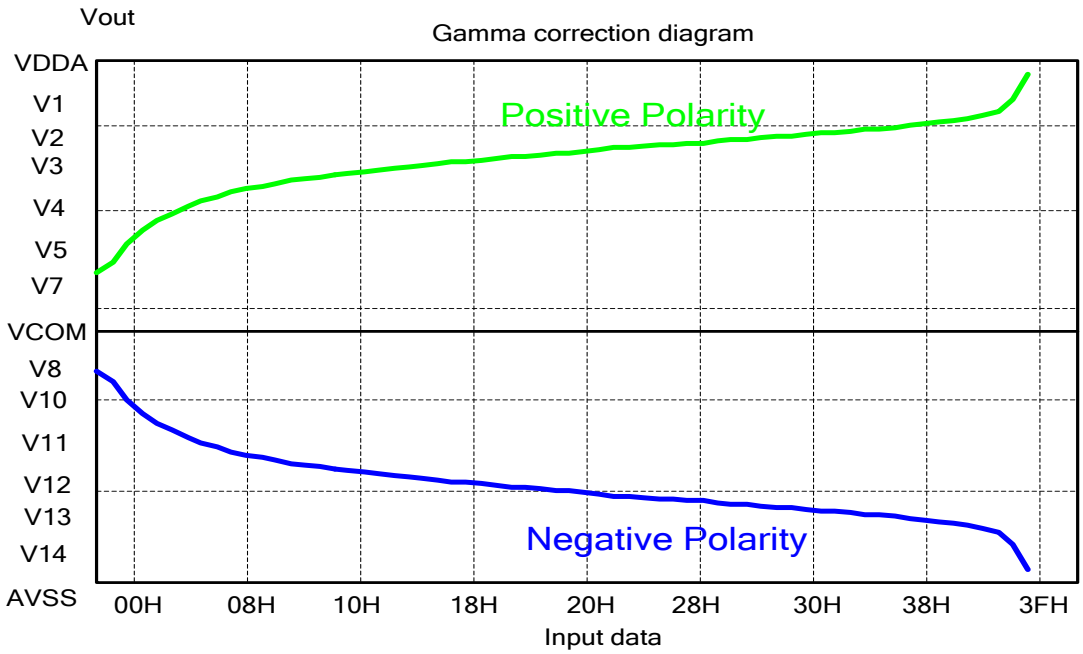
(2) SHLR = 0, left shift

Output	SO[1]	SO[2]	SO[3]	---	SO[1534]	SO[1535]	SO[1536]
Order	First data			←	Last data		
Odd Line /Gn	D07~D00	D27~D20	D17~D10	---	D07~D00	D27~D20	D17~D10
Odd Line /Gn+1	D17~D10	D07~D00	D27~D20	---	D17~D10	D07~D00	D27~D20
Evne Line n	D07~D00	D27~D20	D17~D10	---	D07~D00	D27~D20	D17~D10
Evne Line Gn+1	D17~D10	D07~D00	D27~D20	---	D17~D10	D07~D00	D27~D20

9.6 Input Data VS Output Voltage

The figure below shows the relationship between the input data and the output voltage. Refer to the following pages for the relative resistor values and voltage calculation method.

Gamma Tables very for each customer. Contact ILITEK for more detail information.



Remark: AGND+0.1<V14<V13<V12<V11<V10<V9<V8;V7<V6<V5<V4<V3<V2<V1< AVDD-0.1

9.7 Input Data and Output Voltage Reference Table

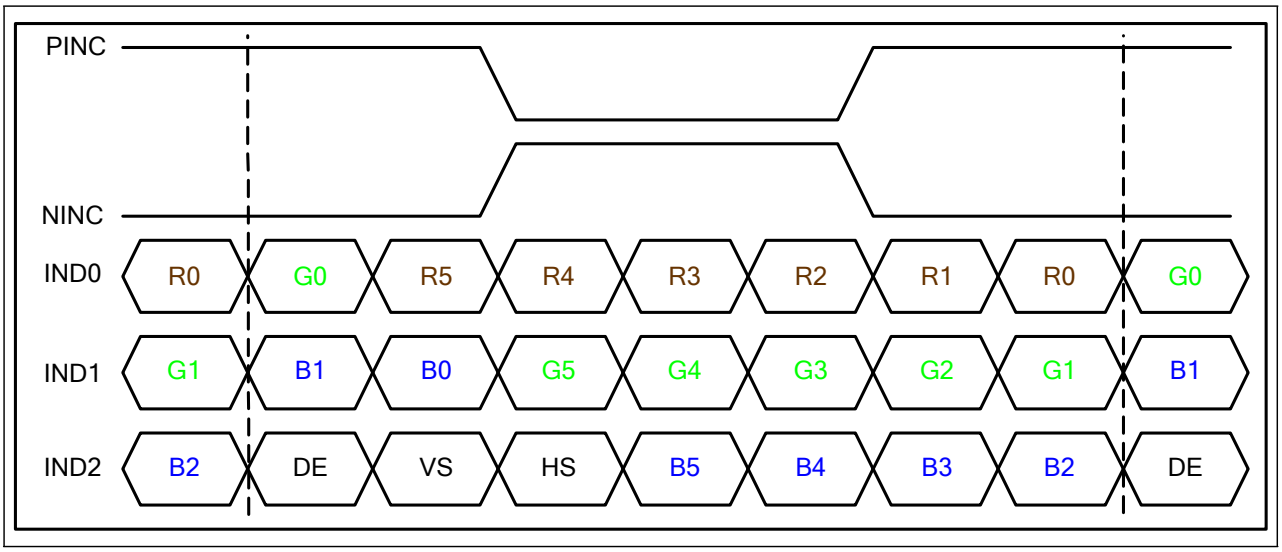
Chip Version	V1	V2	V3	V4	V5	V6	V7	V8	V9	V10	V11	V12	V13	V14	Unit
ILI6150	0.959 *AVDD	0.914 *AVDD	0.773 *AVDD	0.713 *AVDD	0.657 *AVDD	0.533 *AVDD	0.516 *AVDD	0.467 *AVDD	0.431 *AVDD	0.302 *AVDD	0.243 *AVDD	0.183 *AVDD	0.046 *AVDD	0.025 *AVDD	V

Data	Positive Voltage	Negative Voltage	Data	Positive Voltage	Negative Voltage
3FH	V1	V14	1FH	V4	V11
3EH	V2	V13	1EH	V4+(V5-V4)X2/31	V11+(V10-V11)X2/32
3DH	V2+(V3-V2)X69/389	V13+(V12-V13)X71/389	1DH	V4+(V5-V4)X4/31	V11+(V10-V11)X4/32
3CH	V2+(V3-V2)X128/389	V13+(V12-V13)X128/389	1CH	V4+(V5-V4)X6/31	V11+(V10-V11)X6/32
3BH	V2+(V3-V2)X174/389	V13+(V12-V13)X173/389	1BH	V4+(V5-V4)X8/31	V11+(V10-V11)X8/32
3AH	V2+(V3-V2)X208/389	V13+(V12-V13)X207/389	1AH	V4+(V5-V4)X10/31	V11+(V10-V11)X10/32
39H	V2+(V3-V2)X237/389	V13+(V12-V13)X238/389	19H	V4+(V5-V4)X12/31	V11+(V10-V11)X12/32
38H	V2+(V3-V2)X261/389	V13+(V12-V13)X262/389	18H	V4+(V5-V4)X14/31	V11+(V10-V11)X14/32
37H	V2+(V3-V2)X281/389	V13+(V12-V13)X282/389	17H	V4+(V5-V4)X16/31	V11+(V10-V11)X16/32
36H	V2+(V3-V2)X300/389	V13+(V12-V13)X299/389	16H	V4+(V5-V4)X18/31	V11+(V10-V11)X18/32
35H	V2+(V3-V2)X315/389	V13+(V12-V13)X314/389	15H	V4+(V5-V4)X20/31	V11+(V10-V11)X20/32
34H	V2+(V3-V2)X330/389	V13+(V12-V13)X329/389	14H	V4+(V5-V4)X22/31	V11+(V10-V11)X22/32
33H	V2+(V3-V2)X343/389	V13+(V12-V13)X342/389	13H	V4+(V5-V4)X24/31	V11+(V10-V11)X24/32
32H	V2+(V3-V2)X355/389	V13+(V12-V13)X355/389	12H	V4+(V5-V4)X26/31	V11+(V10-V11)X26/32
31H	V2+(V3-V2)X367/389	V13+(V12-V13)X367/389	11H	V4+(V5-V4)X28/31	V11+(V10-V11)X28/32
30H	V2+(V3-V2)X379/389	V13+(V12-V13)X379/389	10H	V4+(V5-V4)X30/31	V11+(V10-V11)X30/32
2FH	V3	V12	0FH	V5	V10
2EH	V3+(V4-V3)X4/44	V12+(V11-V12)X4/52	0EH	V5+(V6-V5)X2/58	V10+(V9-V10)X3/80
2DH	V3+(V4-V3)X7/44	V12+(V11-V12)X8/52	0DH	V5+(V6-V5)X4/58	V10+(V9-V10)X6/80
2CH	V3+(V4-V3)X10/44	V12+(V11-V12)X12/52	0CH	V5+(V6-V5)X6/58	V10+(V9-V10)X9/80
2BH	V3+(V4-V3)X13/44	V12+(V11-V12)X16/52	0BH	V5+(V6-V5)X8/58	V10+(V9-V10)X12/80
2AH	V3+(V4-V3)X16/44	V12+(V11-V12)X19/52	0AH	V5+(V6-V5)X10/58	V10+(V9-V10)X16/80
29H	V3+(V4-V3)X19/44	V12+(V11-V12)X22/52	09H	V5+(V6-V5)X12/58	V10+(V9-V10)X21/80
28H	V3+(V4-V3)X22/44	V12+(V11-V12)X25/52	08H	V5+(V6-V5)X14/58	V10+(V9-V10)X26/80
27H	V3+(V4-V3)X25/44	V12+(V11-V12)X28/52	07H	V5+(V6-V5)X16/58	V10+(V9-V10)X31/80
26H	V3+(V4-V3)X28/44	V12+(V11-V12)X31/52	06H	V5+(V6-V5)X20/58	V10+(V9-V10)X36/80
25H	V3+(V4-V3)X31/44	V12+(V11-V12)X34/52	05H	V5+(V6-V5)X24/58	V10+(V9-V10)X41/80
24H	V3+(V4-V3)X33/44	V12+(V11-V12)X37/52	04H	V5+(V6-V5)X29/58	V10+(V9-V10)X49/80
23H	V3+(V4-V3)X35/44	V12+(V11-V12)X40/52	03H	V5+(V6-V5)X38/58	V10+(V9-V10)X59/80
22H	V3+(V4-V3)X37/44	V12+(V11-V12)X43/52	02H	V5+(V6-V5)X48/58	V10+(V9-V10)X69/80
21H	V3+(V4-V3)X39/44	V12+(V11-V12)X46/52	01H	V6	V9
20H	V3+(V4-V3)X41/44	V12+(V11-V12)X49/52	00H	V7	V8

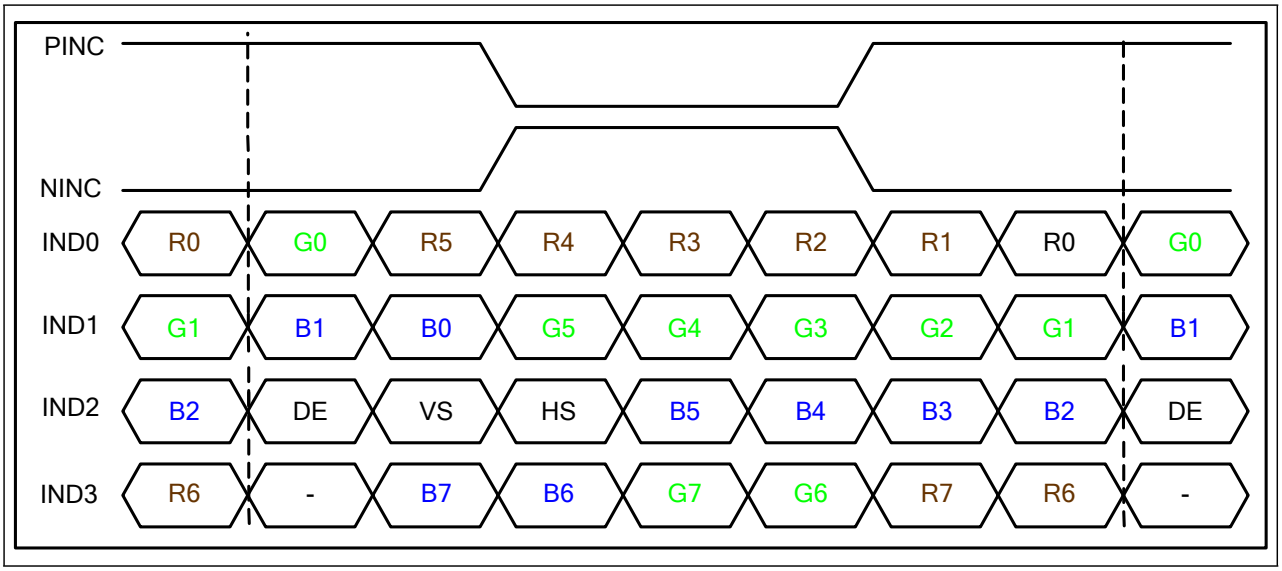
10. Function Description

10.1 Data Input Format for LVDS

6bit LVDS input

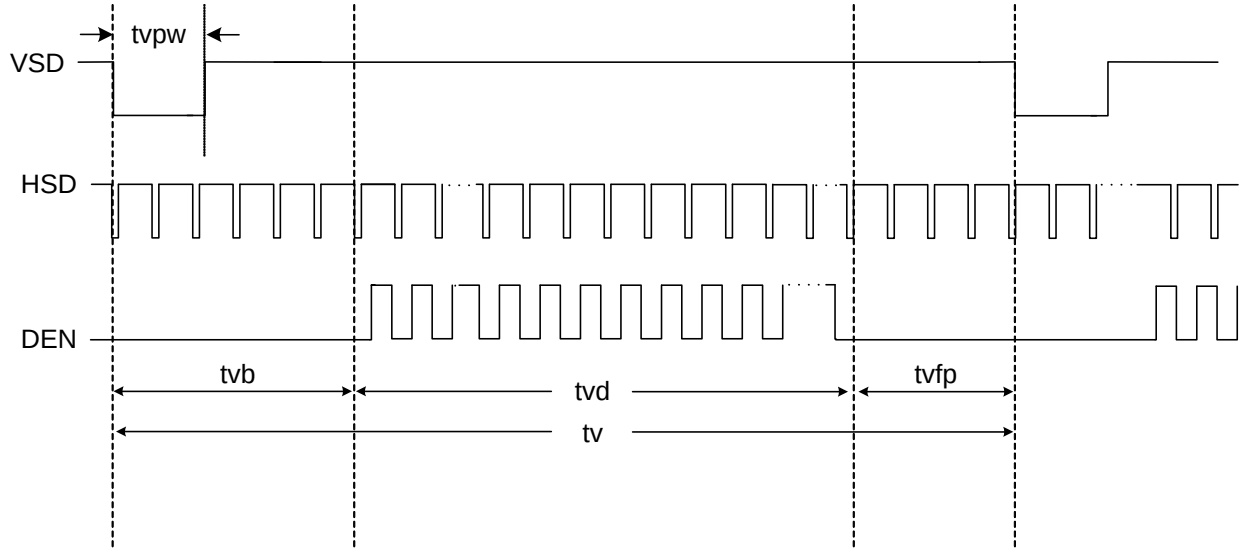


8bit LVDS input

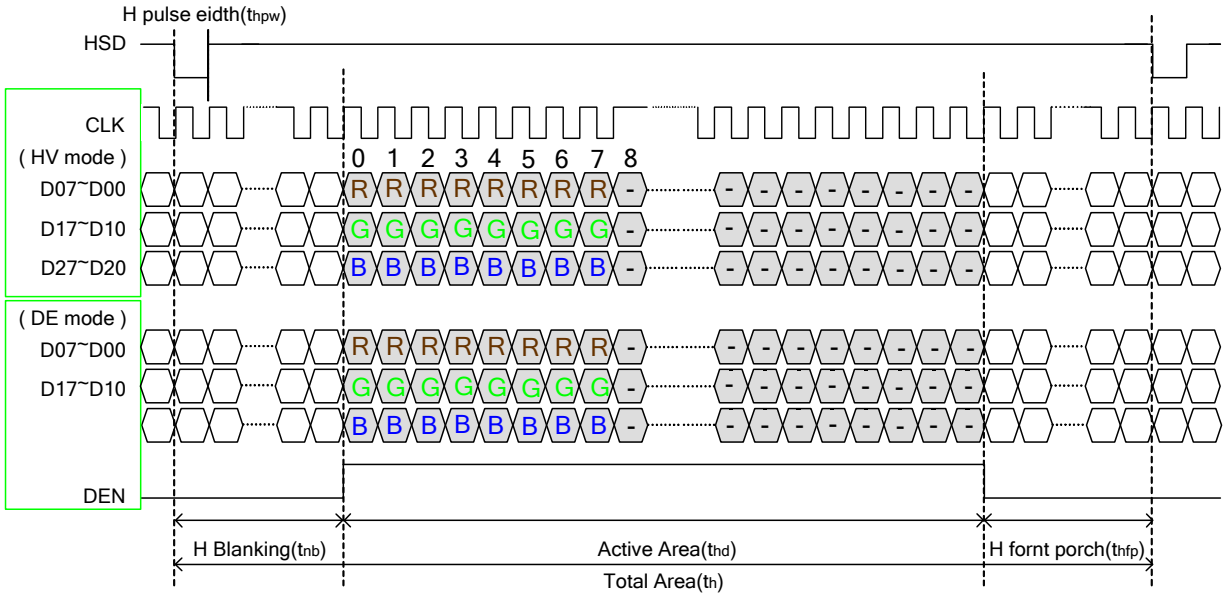


10.2 Data Input Format for TTL

Vertical input timing



Horizontal input timing



10.3 Parallel RGB input timing table

1. 1024x768 panel

DE Mode

Parameter	Symbol	Value			Unit
		Min	Typ.	Max	
DCLK frequency Frame rate = 60Hz	fclk	54.33	65	71	MHz
Horizontal display area	thd		1024		DCLK
HSYNC period time	th	1164	1344	1400	DCLK
HSYNC blanking	thb+thfp	140	320	376	DCLK
Vertical display area	tvd		768		H
VSYNC period time	tv	778	806	845	H
VSYNC blanking	tvb+tvfp	10	38	77	H

HV Mode

a. Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd	1024			DCLK
DCLK frequency Frame rate = 60Hz		fclk	Min	Typ.	Max	
			57	65	70.5	MHz
1 Horizontal Line		th	1200	1344	1400	DCLK
HSYNC pulse width	Min	thpw	1			DCLK
	Typ.		-			
	Max		140			
HSYNC blanking		thb	160	160	160	
HSYNC front porch		thfp	16	160	216	

b. Vertical input timing

Parameter	Symbol	Value			Unit
		Min	Typ.	Max	
Vertical display area	tvd		768		H
VSYNC period time	tv	792	806	840	H
VSYNC pulse width	tvpw	1	-	20	H
VSYNC blanking	tvb	23	23	23	H
VSYNC front porch	tvfp	1	15	49	H

2. 1024x600 panel

DE Mode

Parameter	Symbol	Value			Unit
		Min	Typ.	Max	
DCLK frequency Frame rate = 60Hz	fclk	42.6	51.2	67.2	MHz
Horizontal display area	thd		1024		DCLK
HSYNC period time	th	1164	1344	1400	DCLK
HSYNC blanking	thb+thfp	140	320	376	DCLK
Vertical display area	tvd		600		H
VSYNC period time	tv	610	635	800	H
VSYNC blanking	tvb+tvfp	10	35	200	H

HV Mode

a. Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd	1024			DCLK
DCLK frequency Frame rate = 60Hz		fclk	Min	Typ.	Max	
			44.9	51.2	63	MHz
1 Horizontal Line		th	1200	1344	1400	DCLK
HSYNC pulse width	Min	thpw	1			DCLK
	Typ.		-			
	Max		140			
HSYNC blanking		thb	160	160	160	
HSYNC front porch		thfp	16	160	216	

b. Vertical input timing

Parameter	Symbol	Value			Unit
		Min	Typ.	Max	
Vertical display area	tvd		600		H
VSYNC period time	tv	624	635	750	H
VSYNC pulse width	tvpw	1	-	20	H
VSYNC blanking	tvb	23	23	23	H
VSYNC front porch	tvfp	1	12	127	H

3. 800x600 panel

DE Mode

Parameter	Symbol	Value			Unit
		Min	Typ.	Max	
DCLK frequency Frame rate = 60Hz	fclk	34.4	39.6	62.4	MHz
Horizontal display area	thd		800		DCLK
HSYNC period time	th	940	1000	1300	DCLK
HSYNC blanking	thb+thfp	140	200	500	DCLK
Vertical display area	tvd		600		H
VSYNC period time	tv	610	660	800	H
VSYNC blanking	tvb+tvfp	10	60	200	H

HV Mode

a. Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd	800			DCLK
DCLK frequency Frame rate = 60Hz		fclk	Min	Typ.	Max	
			34.5	39.6	50.4	MHz
1 Horizontal Line		th	900	1000	1200	DCLK
HSYNC pulse width	Min	thpw	1			DCLK
	Typ.		-			
	Max		40			
HSYNC blanking		thb	88	88	88	
HSYNC front porch		thfp	12	112	312	

b. Vertical input timing

Parameter	Symbol	Value			Unit
		Min	Typ.	Max	
Vertical display area	tvd		600		H
VSYNC period time	tv	640	660	700	H
VSYNC pulse width	tvpw	1	-	20	H
VSYNC blanking	tvb	39	39	39	H
VSYNC front porch	tvfp	1	21	61	H

4. 800x480 panel

DE Mode

Parameter	Symbol	Value			Unit
		Min	Typ.	Max	
DCLK frequency Frame rate = 60Hz	fclk	27.64	29.2	54.6	MHz
Horizontal display area	thd		800		DCLK
HSYNC period time	th	940	928	1300	DCLK
HSYNC blanking	thb+thfp	140	128	500	DCLK
Vertical display area	tvd		480		H
VSYNC period time	tv	490	525	700	H
VSYNC blanking	tvb+tvfp	10	45	220	H

HV Mode

a. Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd		800		DCLK
DCLK frequency Frame rate = 60Hz		fclk	Min	Typ.	Max	
			27.7	29.2	39.6	MHz
1 Horizontal Line		th	900	928	1100	DCLK
HSYNC pulse width	Min	thpw	1			DCLK
	Typ.		-			
	Max		40			
HSYNC blanking		thb	88	88	88	
HSYNC front porch		thfp	12	40	212	

b. Vertical input timing

Parameter	Symbol	Value			Unit
		Min	Typ.	Max	
Vertical display area	tvd		480		H
VSYNC period time	tv	513	525	600	H
VSYNC pulse width	tvpw	1	-	3	H
VSYNC blanking	tvb	32	32	32	H
VSYNC front porch	tvfp	1	13	88	H

5. 960x540 panel

DE Mode

Parameter	Symbol	Value			Unit
		Min	Typ.	Max	
DCLK frequency Frame rate = 60Hz	fclk	37.82	38.6	43.2	MHz
Horizontal display area	thd		960		DCLK
HSYNC period time	th	1100	1100	1200	DCLK
HSYNC blanking	thb+thfp	140	140	240	DCLK
Vertical display area	tvd		540		H
VSYNC period time	tv	573	585	600	H
VSYNC blanking	tvb+tvfp	33	45	60	H

HV Mode

a. Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd		960		DCLK
DCLK frequency Frame rate = 60Hz		fclk	Min	Typ.	Max	
			36.4	38.6	43.2	MHz
1 Horizontal Line		th	1060	1100	1200	DCLK
HSYNC pulse width	Min	thpw		1		DCLK
	Typ.			--		
	Max			20		
HSYNC blanking		thb	88	88	88	
HSYNC front porch		thfp	12	52	152	

b. Vertical input timing

Parameter	Symbol	Value			Unit
		Min	Typ.	Max	
Vertical display area	tvd		540		H
VSYNC period time	tv	573	585	600	H
VSYNC pulse width	tvpw	1	--	3	H
VSYNC blanking	tvb	32	32	32	H
VSYNC front porch	tvfp	1	13	88	H

6. 960x640 panel

DE Mode

Parameter	Symbol	Value			Unit
		Min	Typ.	Max	
DCLK frequency Frame rate = 60Hz	fclk	44.89	45.87	56.60	MHz
Horizontal display area	thd		960		DCLK
HSYNC period time	th	1100	1100	1200	DCLK
HSYNC blanking	thb+thfp	140	140	240	DCLK
Vertical display area	tvd		640		H
VSYNC period time	tv	680	695	786	H
VSYNC blanking	tvb+tvfp	40	55	146	H

HV Mode

a. Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd		960		DCLK
DCLK frequency Frame rate = 60Hz		fclk	Min	Typ.	Max	
			43.25	45.87	55.30	MHz
1 Horizontal Line		th	1060	1100	1200	DCLK
HSYNC pulse width	Min	thpw		1		DCLK
	Typ.			--		
	Max			20		
HSYNC blanking		thb	88	88	88	
HSYNC front porch		thfp	12	52	152	

b. Vertical input timing

Parameter	Symbol	Value			Unit
		Min	Typ.	Max	
Vertical display area	tvd		640		H
VSYNC period time	tv	680	695	786	H
VSYNC pulse width	tvpw	1	-	20	H
VSYNC blanking	tvb	39	39	39	H
VSYNC front porch	tvfp	1	16	107	H

7. 600x1024 panel

DE Mode

Parameter	Symbol	Value			Unit
		Min	Typ.	Max	
DCLK frequency Frame rate = 60Hz	fclk	45.47	50.97	65.76	MHz
Horizontal display area	thd		600		DCLK
HSYNC period time	th	740	800	1000	DCLK
HSYNC blanking	thb+thfp	140	200	400	DCLK
Vertical display area	tvd		1024		H
VSYNC period time	tv	1048	1062	1096	H
VSYNC blanking	tvb+tvfp	24	38	72	H

HV Mode

a. Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd	600			DCLK
DCLK frequency Frame rate = 60Hz		fclk	Min	Typ.	Max	
			44	50.97	65.76	MHz
1 Horizontal Line		th	700	800	1000	DCLK
HSYNC pulse width	Min	thpw	1			DCLK
	Typ.		--			
	Max		40			
HSYNC blanking		thb	88	88	88	
HSYNC front porch		thfp	12	112	312	

b. Vertical input timing

Parameter	Symbol	Value			Unit
		Min	Typ.	Max	
Vertical display area	tvd		1024		H
VSYNC period time	tv	1048	1062	1096	H
VSYNC pulse width	tvpw	1	-	20	H
VSYNC blanking	tvb	23	23	23	H
VSYNC front porch	tvfp	1	15	49	H

11. Absolute Maximum Rating

Description	Min	Max	Unit
Logic supply voltage, VDD Digital input voltage	-0.5	5	V
Analog supply voltage, AVDD Gamma voltage , V1~V14 SO[1] ~ SO[1536]	-0.5	15	V

TEMPREATURE

Description	Min	Max	Unit
Operating temperature	-20	85	°C
Storage temperature	-55	125	°C

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or under any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

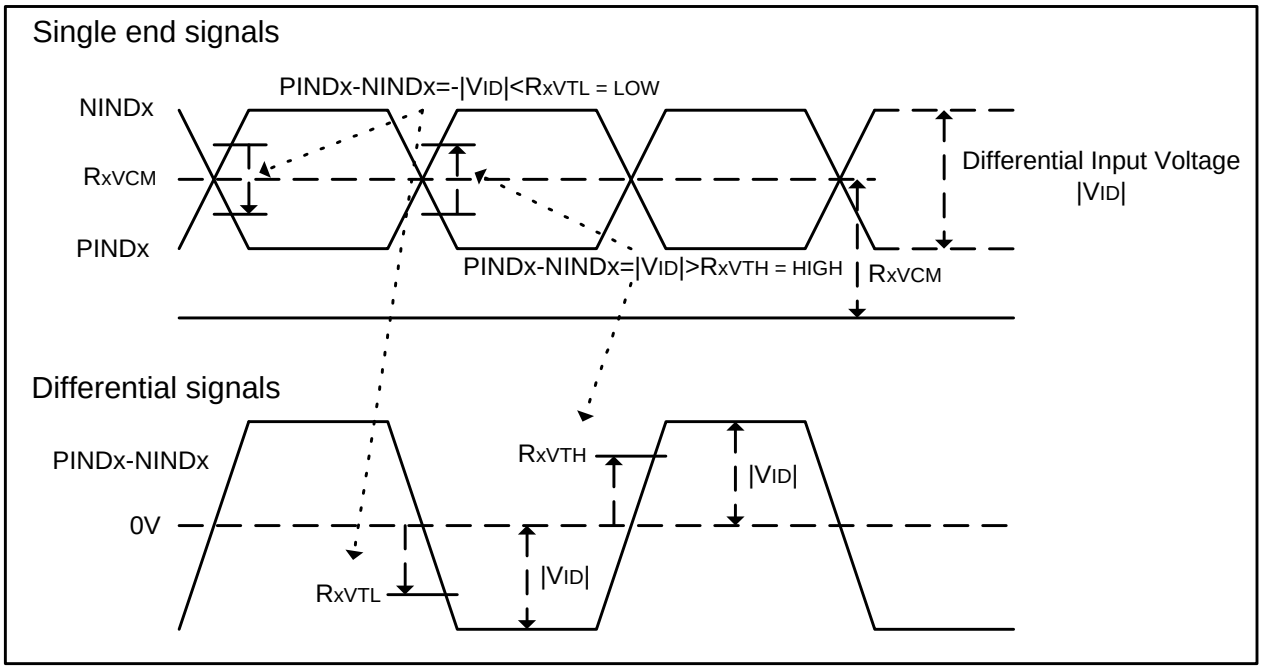
11.1 DC Electrical Characteristics

TTL mode
(VDD= 2.3 to 3.6V, AVDD= 8 to 13.5V, GND=AGND= 0V, TA= -20 to +85°C)

Parameter	Symbol	Min	Typ.	Max	Unit	Conditions
Power Supply voltage	VDD	2.3	-	3.6	V	--
Power Supply voltage	AVDD	8	-	13.5	V	--
Power Supply voltage	AVDDL	8	-	13.5	V	Full Range Application
Power Supply voltage		4	-	6.75	V	Half AVDD Application
Power Supply voltage	AGNDH	0	0	0	V	Full Range Application
Power Supply voltage		4	-	6.75	V	Half AVDD Application
Low level input voltage	Vil	0	0	0.3xVDD	V	For the digital circuit
High level input voltage	Vih	0.7xVDD	VDD	VDD	V	For the digital circuit
Input leakage current	Ii	-	-	+/-1	uA	For the digital circuit
High level output voltage	Voh	VDD-0.4	-	-	V	Ioh=-400A
Low level output voltage	Vol	-	-	GND+0.4	V	Iol=+400A
Pull low / high resistor	Ri	200K	250K	300K	ohm	For the digital input pin,VDD=3.3V
Digital Operating Current	Idd	-	3.8	5	mA	Fclk=65MHz,FLD=50K,VDD=3.3V
Digital Standby current	Ist1	-	55	100	uA	Clock and all function are stopped
Analog Operating Current	Idda	-	10	12	mA	No load,Fclk=65MHz,FLD=50KHz AVDD=10V,V1=8V,V14=0.4V
Analog Standby current	Ist2	-	10	50	uA	No load, Clock and all functions are Stopped
Input level of V1~V7	Vref1	0.4xAVDD	-	AVDD-0.1	V	Gamma correction voltage input
Input level of V8~V14	Vref2	0.1	-	0.6xAVDD	V	Gamma correction voltage input
Output Voltage deviatio	Vod1	-	+/-20	+/-35	mV	Vo=AGND+0.1V~AGND+0.5V and Vo=AVDD-0.5V~AVDD-0.1V
Output Voltage deviation	Vod2	-	+/-15	+/-20	mV	Vo=AGND+0.5V~AVDD-0.5V
Output Voltage Offset Between Chips	Voc	-	-	+/-20	V	Vo=AGND+0.5V~AVDD-0.5V
Dynamic Range of Output	Vdr	0.1	-	AVDD-0.1	V	S1~S1536
Sinking Range of Output	IOLy	80	-	-	uA	S1~S1536; Vo=0.1V v.s 1.0V AVDD=13.5V
Driving Range of Output	IOHy	80	-	-	uA	S1~S1536; Vo=13.4V v.s 12.5V AVDD=13.5V
Resistance of Gamma Table	Rg	0.7xRn	1.0xRn	1.3xRn	ohm	Rn: internal gamma resistor

LVDS mode (Receiver Differential Input: PIND0~PIND3, NIND0~NIND3, PINC, NINC)

Parameter	Symbol	Min	Typ.	Max	Unit	Conditions
Differential input high threshold voltage	RxVTH	0.1	0.2	|VID|	V	RxVCM=1.2V
Differential input low threshold voltage	RxVTL	-|VID|	-0.2	-0.1	V	
Input voltage range (singled-end)	RxVIN	0	1.2±0.4	2.4	V	
Differential input common mode voltage	RxVCM	|VID|/2	1.2	2.1-|VID|/2	V	
Differential input voltage	|VID|	0.2	0.4	0.6	V	
Differential input leakage current	RVxliz	-10	0	+10	uA	
LVDS Digital Operating Current	Iddlvds	8	22	30	mA	Fclk=65MHz,VDD=3.3V
LVDS Digital Standby Current	Istlvds	0	200	300	uA	Clock & all Functions are stopped


Single end signals
PINDx-NINDx=-|VID|<RxVTL = LOW
NINDx
RxVCM
PINDx
Differential Input Voltage
|VID|
PINDx-NINDx=|VID|>RxVTH = HIGH
RxVCM
Differential signals
PINDx-NINDx
0V
RxVTH
|VID|
|VID|
RxVTL

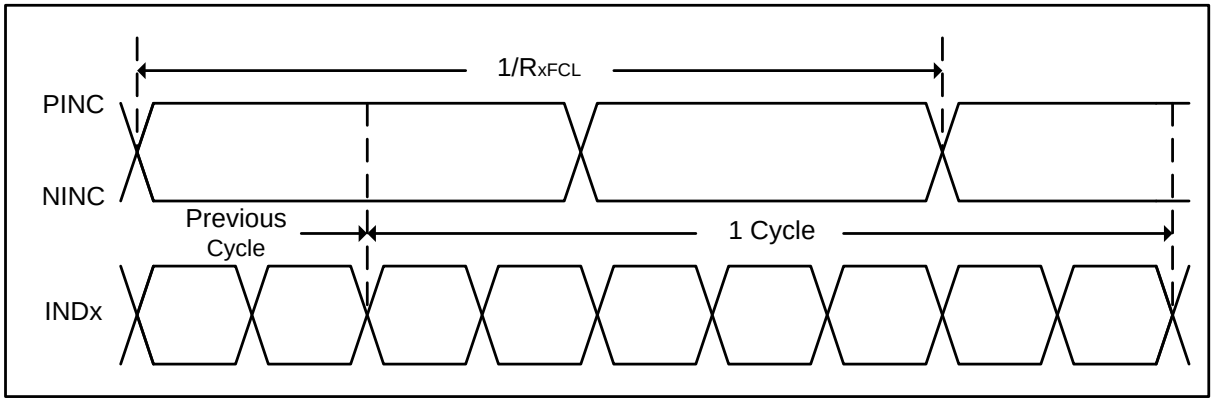
11.2 AC Electrical Characteristics

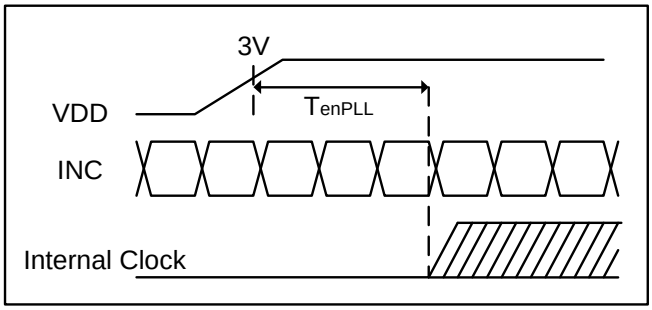
TTL mode(VDD= 2.3 to 3.6V, AVDD= 8 to 13.5V, GND=AGND= 0V, TA= -20 to +85°C)

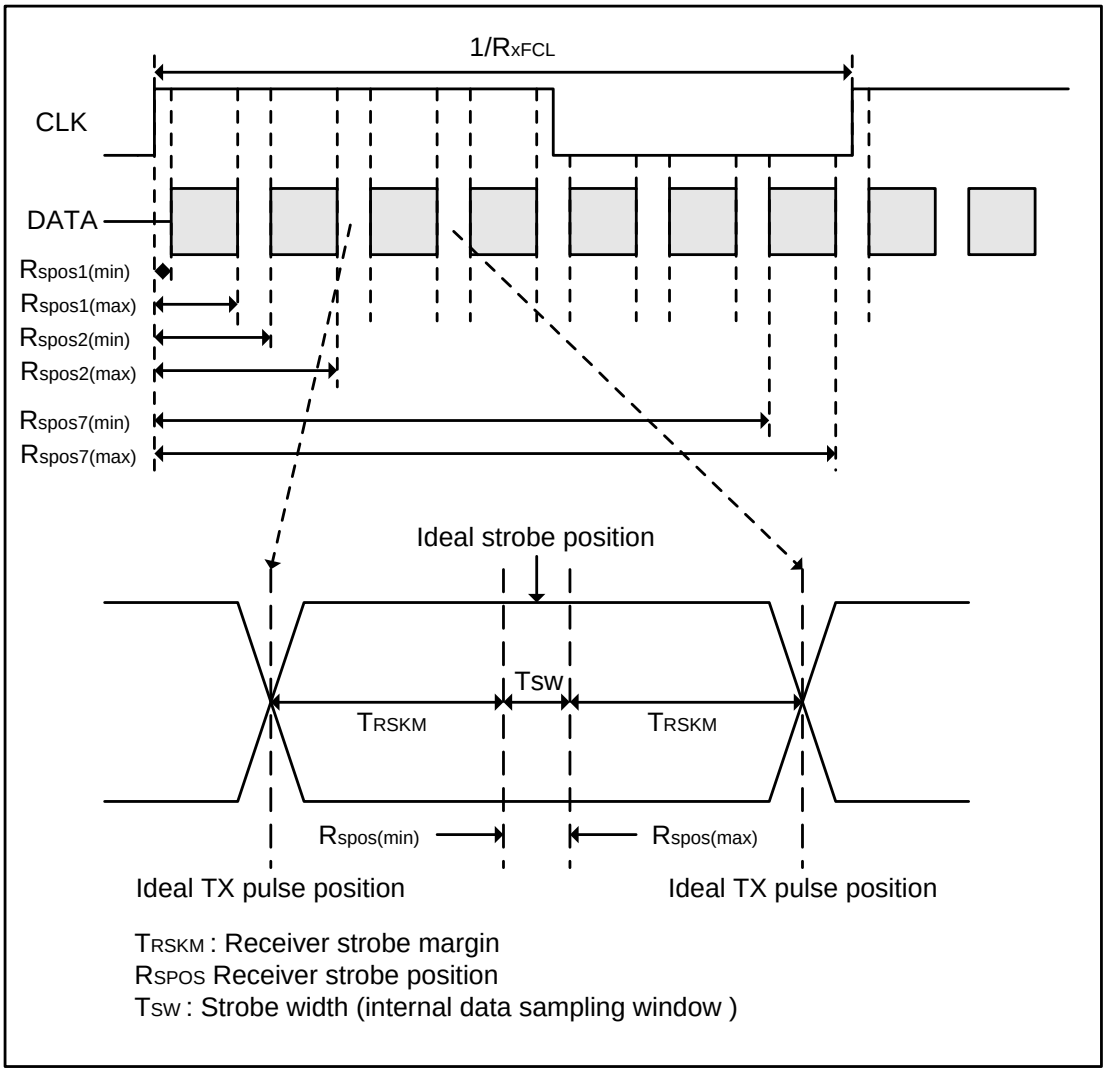
Parameter	Symbol	Min	Typ.	Max	Unit	Conditions
VDD power on Slew rate	TPOR	-	-	20	ms	From 0V to 0.9VDD
RSTB pulse width	TRst	50	-	-	us	DCLK=65MHz
DCLK cycle time	Tcph	14			ns	
DCLK pulse duty	Tcwh	40	50	60	%	
VSD setup time	Tvst	5	-	-	ns	
VSD hold time	Tvhd	5	-	-	ns	
HSD setup time	Thst	5	-	-	ns	
HSD hold time	Thhd	5	-	-	ns	
Data setup time	Tdsu	5	-	-	ns	D0[7:0],D1[7:0],D2[7:0] to DCLK
Data hold time	Tdhu	5	-	-	ns	D0[7:0],D1[7:0],D2[7:0] to DCLK
OE setup time	Tesu	5	-	-	ns	
OE hold time	Tehd	5	-	-	ns	
Output stable time	Tsst	-	-	6	us	10% to 90% target Voltage. CL=90pF,R=10K ohm (Cascade)
				3		Dual gate

LVDS mode

Parameter	Symbol	Min	Typ.	Max	Unit	Conditions
Clock frequency	RxFCLK	26.2	51.2	71	MHz	Typical value for 1024*600 resolution
Input data skew margin	TRSKM	500	500	1/(2*RxFCLK)	ps	|VID|=400mv RxVCM=1.2V RxFCLK=71MHz VDD_LVDS=3.3V
Clock high time	TLVCH	4/(7xRxFCLK)			ns	
Clock low time	TLVCL	3/(7xRxFCLK)			ns	
VSD setup time	TenPLL	0<TenPLL<150			us	







SSC torence of LVDS receiver

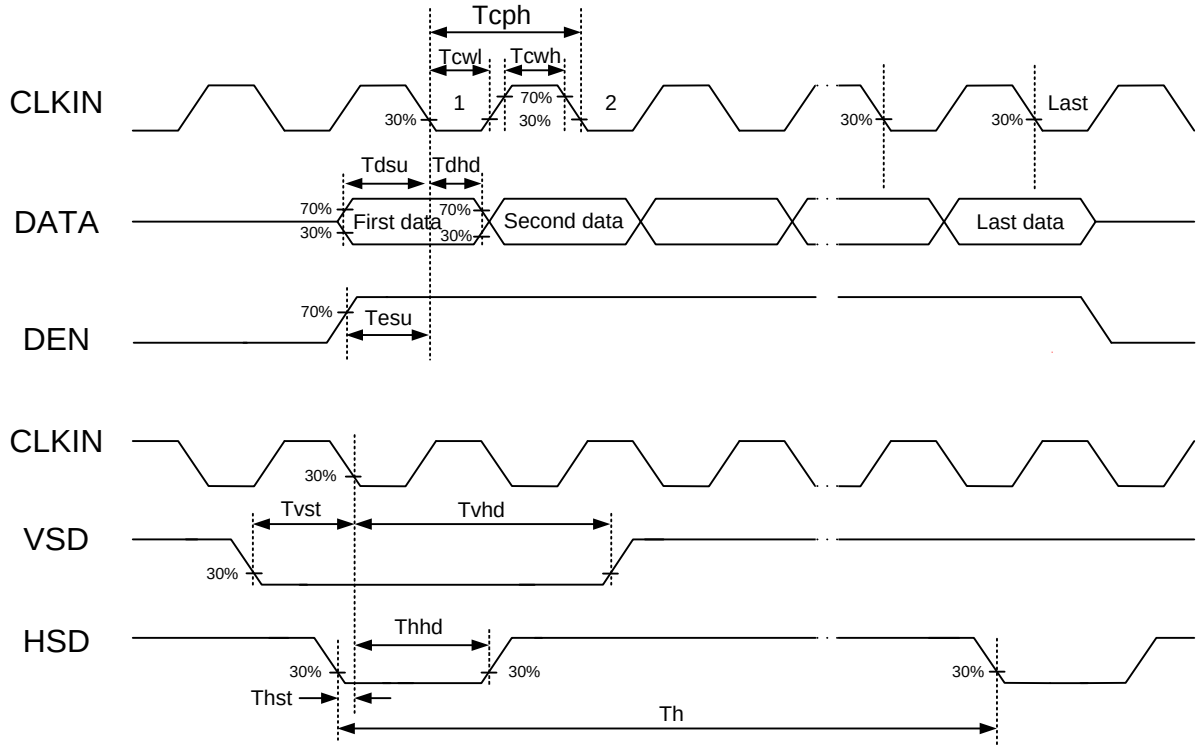
symbol	parameter	condition	Min	Typ.	Max	Units
SSCMF	Modulation Freq.		23		93	KHz
SSCMR	Modulation Rate	LVDS clock=71MHz center spread			+/-3	%

Output timing table

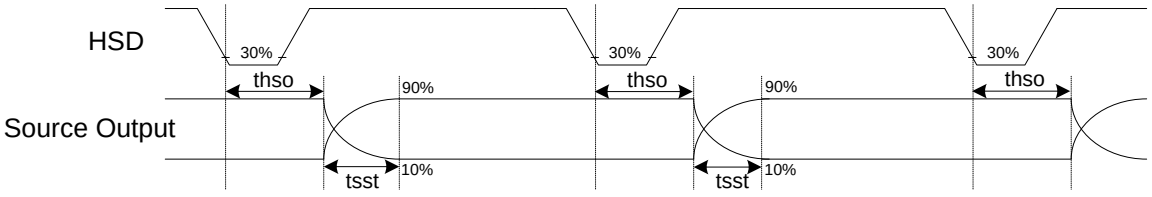
parameter	Symbol	Min	Typ.	Max	Units	condition
DCLK Frequency	Fclk	-	65	71	MHz	VDD=2.3V~3.6V
DCLK Cycle Time	Tclk	14.1	15.4	-	ns	
DCLK Pulse Duty	Tcwh	40	50	60	%	Tclk
Time from HSD to Source Output	Thso	-	64	-	DCLK	
Time from HSD to LD	Thld	-	64	-	DCLK	
Time from HSD to STV	Thstv	-	2	-	DCLK	
Time from HSD to CKV	Thckv	-	20	-	DCLK	
Time from HSD to OEV	Thoev	-	4		DCLK	
LD Pulse Width	Twld	-	10	-	DCLK	
CKV Pulse Width	Twckv	-	66	-	DCLK	
OEV Pulse Width	Twoev	-	74	-	DCLK	

12. Timing Diagram

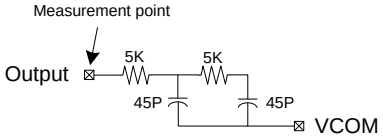
12.1 input Clock and Data Timing Diagram



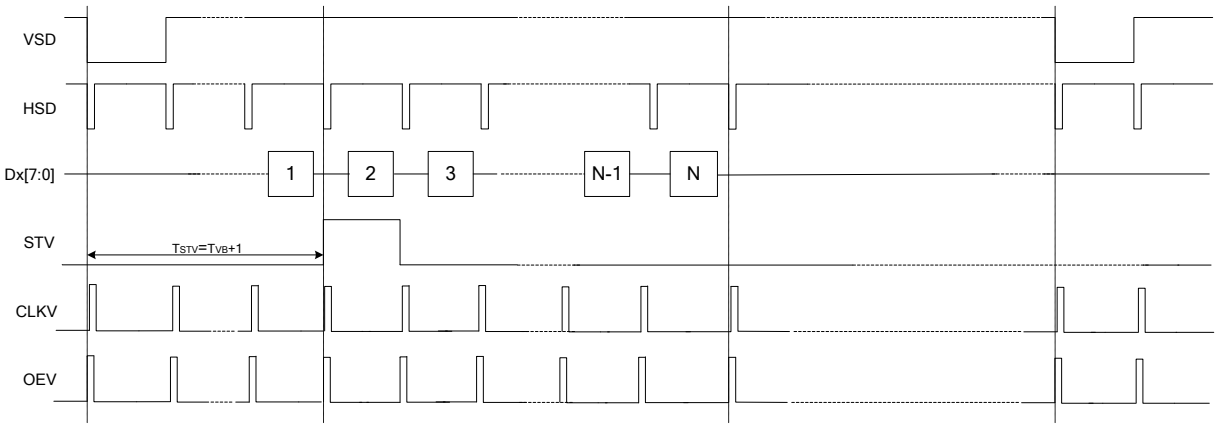
12.2 Source Output Timing Diagram (cascade)



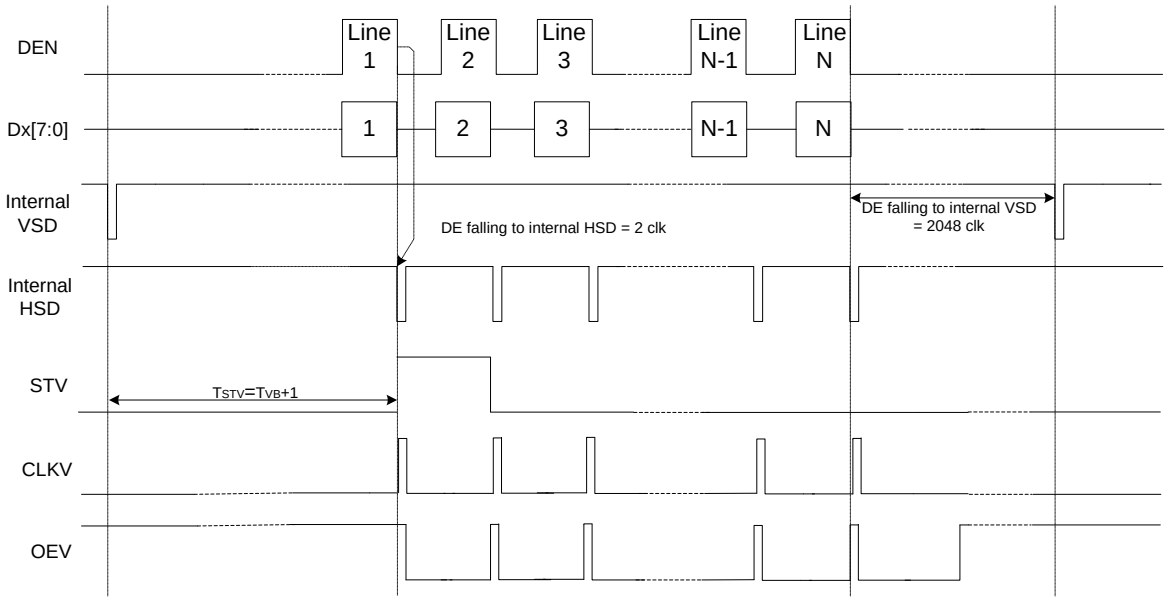
Output load condition :



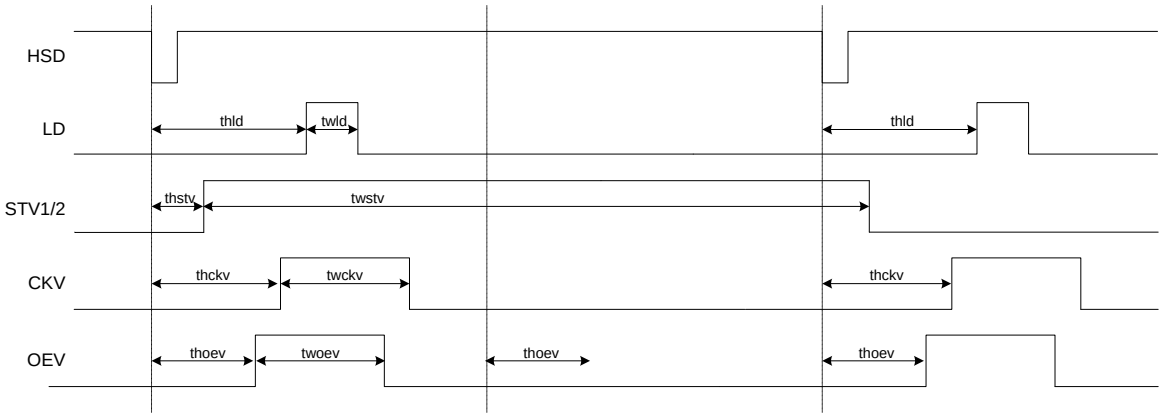
12.3 Vertical Timing Diagram HV (cascade)



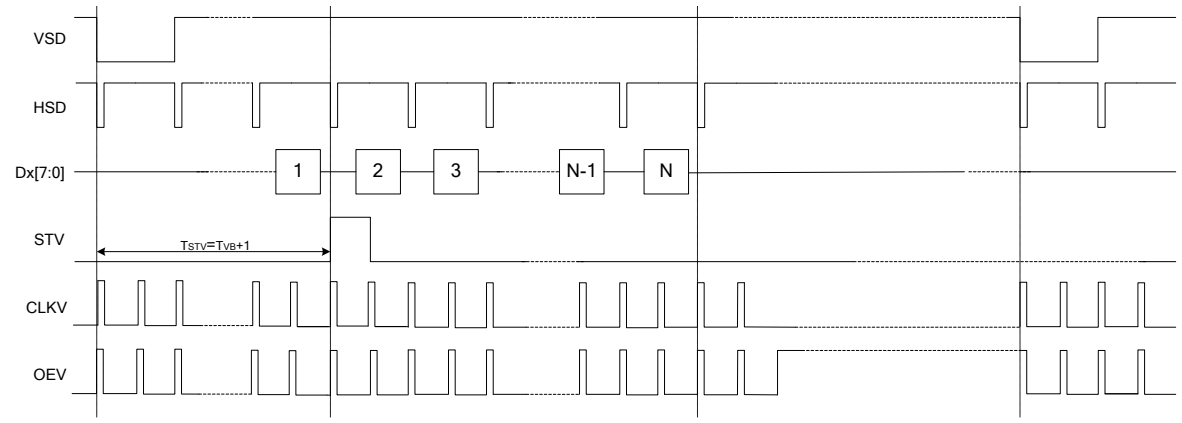
12.4 Vertical Timing Diagram DE (cascade)



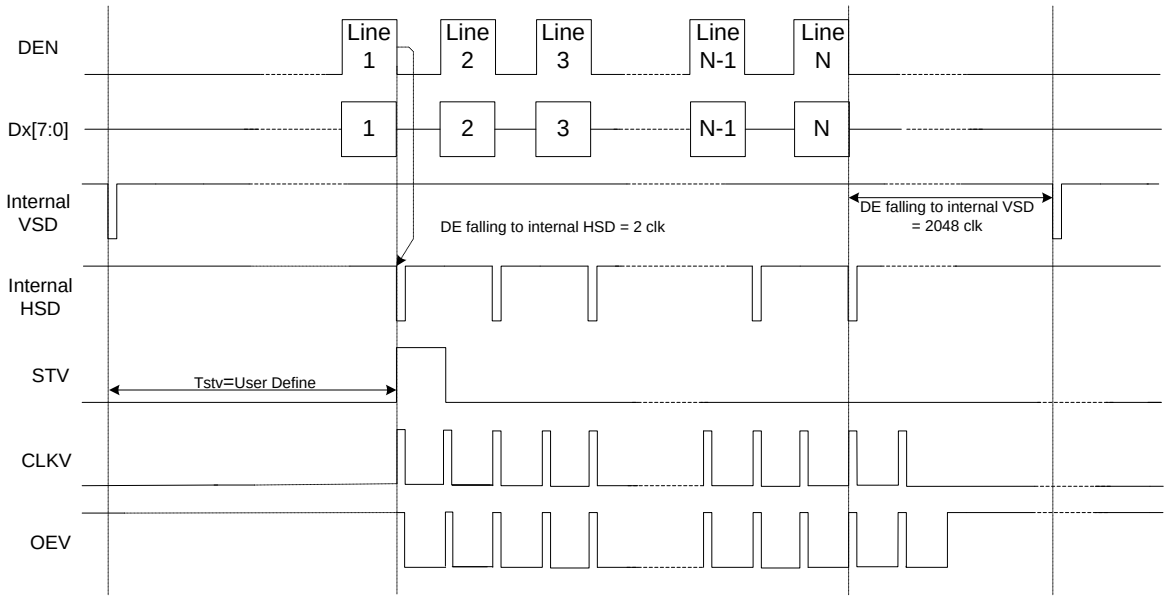
12.5 Gate output Timing Diagram HV (cascade)



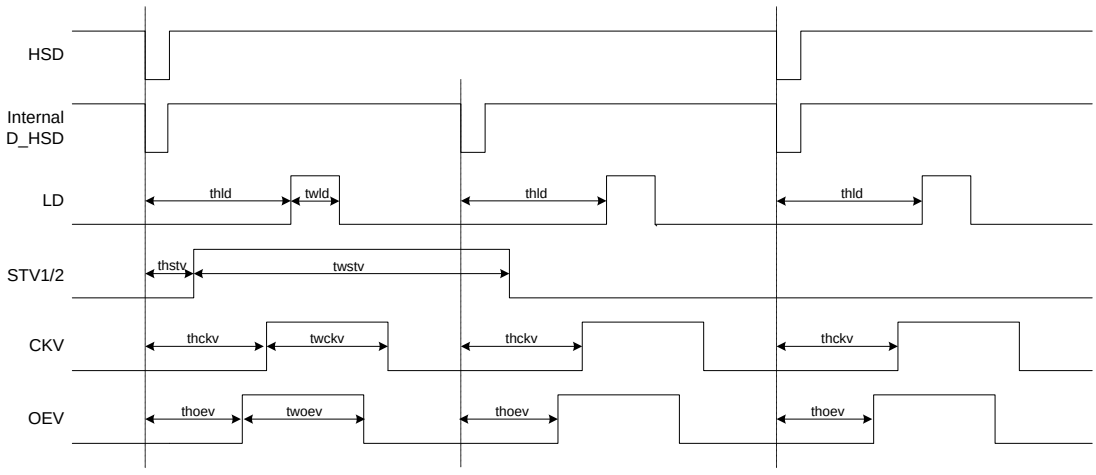
12.6 Vertical Timing Diagram HV (dual gate)



12.7 Vertical Timing Diagram DE (dual gate)



12.8 Gate output Timing Diagram HV (dual gate)

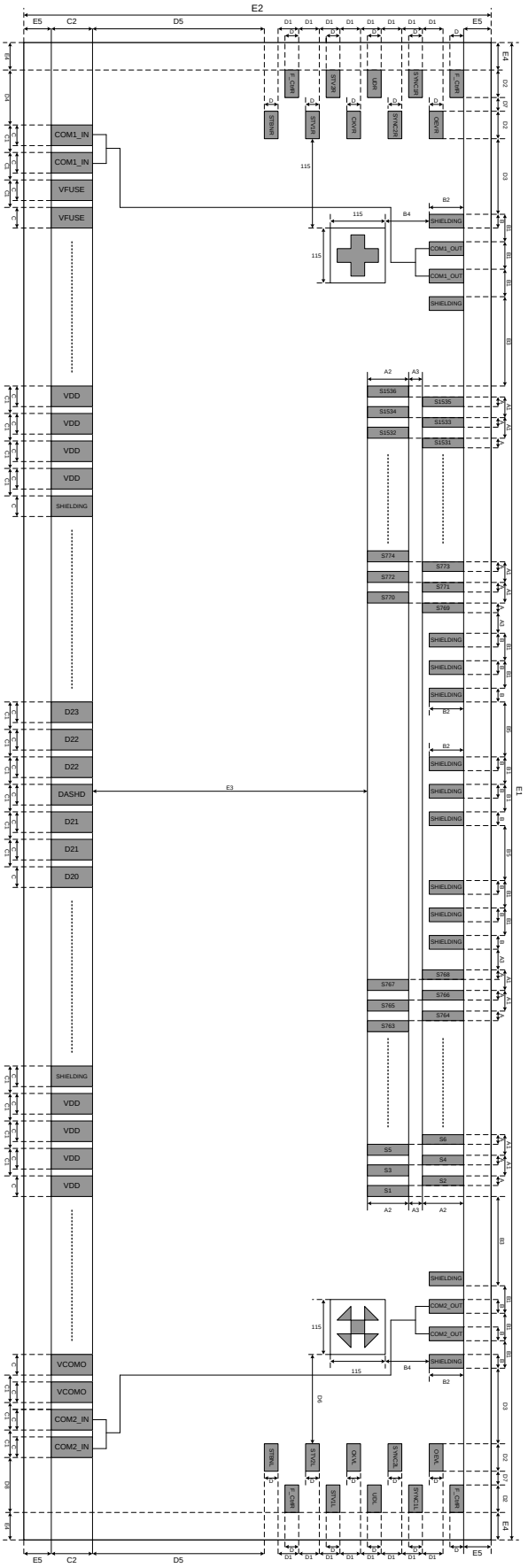


12.9 Internal VCO OSC timing Specification

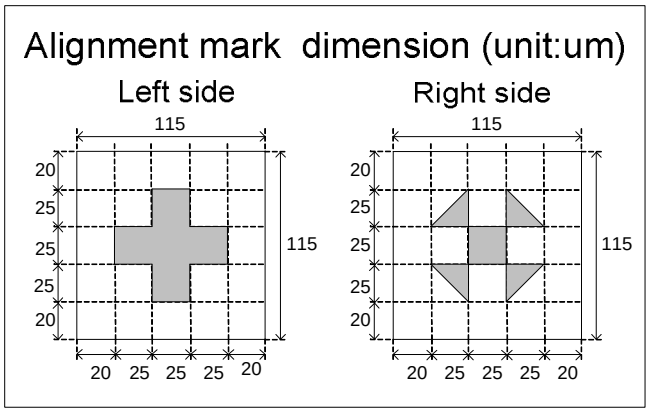
(At GND = 0V, TA= +25°C)

Condition	Min	Typ	Max	Unit
VDD=2.7V	25.2	28	30.8	MHz
VDD=3.3V	27.9	31	34.1	

13. Pad outline Dimension (Bump Side)



13.1 Alignment Mark



13.2 Pad Information

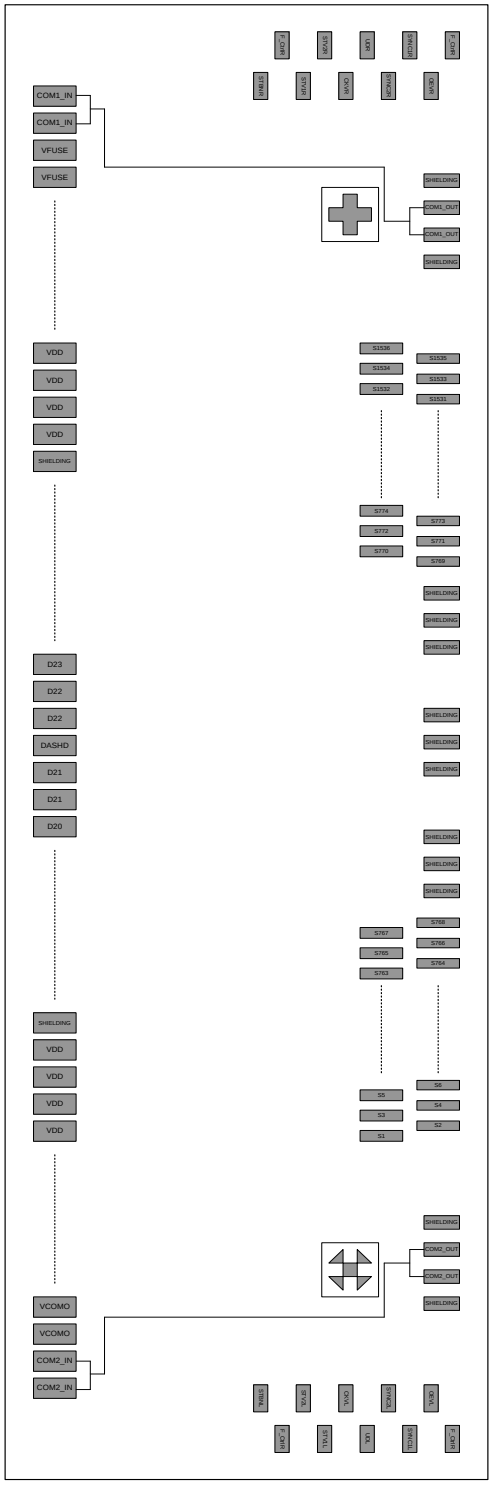
Symbol	Dimension in um		Symbol	Dimension in um
A	13		D	28
A1	30		D1	40
A2	98		D2	78
A3	32		D3	47
			D4	33
B	28		D5	98
B1	50		D6	75
B2	68		D7	22
B3	50		D8	53
B4	51			
B5	277		E1	24980
			E2	680
C	63		E3	258
C1	85		E4	48
C2	98		E5	48

Note:

A. Chip dimension include scribe line.

B. **Bump Height 9um.**

14. Pad Coordinate



14.1 Pad Location

Pad	Name	X	Y	Pad	Name	X	Y	Pad	Name	X	Y
1	COM1_IN	-12377.5	-243	52	HFRC	-8042.5	-243	103	V7	-3707.5	-243
2	COM1_IN	-12292.5	-243	53	TPI[4]	-7957.5	-243	104	GAMH	-3622.5	-243
3	VFUSE	-12207.5	-243	54	TPI[4]	-7872.5	-243	105	GAMH	-3537.5	-243
4	VFUSE	-12122.5	-243	55	FRAME	-7787.5	-243	106	SHIELDING	-3452.5	-243
5	VFUSE	-12037.5	-243	56	FRAME	-7702.5	-243	107	DASHD	-3367.5	-243
6	VFUSE	-11952.5	-243	57	SEL[0]	-7617.5	-243	108	VSD	-3282.5	-243
7	SHIELDING	-11867.5	-243	58	SEL[0]	-7532.5	-243	109	DASHD	-3197.5	-243
8	AGND	-11782.5	-243	59	SEL[1]	-7447.5	-243	110	HSD	-3112.5	-243
9	AGND	-11697.5	-243	60	SEL[1]	-7362.5	-243	111	DASHD	-3027.5	-243
10	AGND	-11612.5	-243	61	CSB	-7277.5	-243	112	DEN	-2942.5	-243
11	AGND	-11527.5	-243	62	CSB	-7192.5	-243	113	GND_LVDS	-2857.5	-243
12	SHIELDING	-11442.5	-243	63	SHIELDING	-7107.5	-243	114	GND_LVDS	-2772.5	-243
13	AVDD	-11357.5	-243	64	SDA	-7022.5	-243	115	GND_LVDS	-2687.5	-243
14	AVDD	-11272.5	-243	65	SDA	-6937.5	-243	116	GND_LVDS	-2602.5	-243
15	AVDD	-11187.5	-243	66	SHIELDING	-6852.5	-243	117	D27	-2517.5	-243
16	AVDD	-11102.5	-243	67	SCL	-6767.5	-243	118	D26	-2432.5	-243
17	SHIELDING	-11017.5	-243	68	SCL	-6682.5	-243	119	DASHD	-2347.5	-243
18	GND	-10932.5	-243	69	SHIELDING	-6597.5	-243	120	D25	-2262.5	-243
19	GND	-10847.5	-243	70	VDD	-6512.5	-243	121	D24	-2177.5	-243
20	GND	-10762.5	-243	71	VDD	-6427.5	-243	122	DASHD	-2092.5	-243
21	GND	-10677.5	-243	72	VDD	-6342.5	-243	123	D23	-2007.5	-243
22	SHIELDING	-10592.5	-243	73	VDD	-6257.5	-243	124	D22	-1922.5	-243
23	VDD	-10507.5	-243	74	SHIELDING	-6172.5	-243	125	DASHD	-1837.5	-243
24	VDD	-10422.5	-243	75	GND	-6087.5	-243	126	D21	-1752.5	-243
25	VDD	-10337.5	-243	76	GND	-6002.5	-243	127	D20	-1667.5	-243
26	VDD	-10252.5	-243	77	GND	-5917.5	-243	128	DASHD	-1582.5	-243
27	TPO[10]	-10167.5	-243	78	GND	-5832.5	-243	129	DCLK	-1497.5	-243
28	TPO[10]	-10082.5	-243	79	SHIELDING	-5747.5	-243	130	NINC	-1412.5	-243
29	TPO[9]	-9997.5	-243	80	AVDDL	-5662.5	-243	131	DASHD	-1327.5	-243
30	TPO[9]	-9912.5	-243	81	AVDDL	-5577.5	-243	132	VDD_LVDS	-1242.5	-243
31	TPO[8]	-9827.5	-243	82	AVDDL	-5492.5	-243	133	VDD_LVDS	-1157.5	-243
32	TPO[8]	-9742.5	-243	83	AVDDL	-5407.5	-243	134	VDD_LVDS	-1072.5	-243
33	TPO[7]	-9657.5	-243	84	SHIELDING	-5322.5	-243	135	VDD_LVDS	-987.5	-243
34	TPO[7]	-9572.5	-243	85	AGNDH	-5237.5	-243	136	REV	-902.5	-243
35	TPO[6]	-9487.5	-243	86	AGNDH	-5152.5	-243	137	DASHD	-817.5	-243
36	TPO[6]	-9402.5	-243	87	AGNDH	-5067.5	-243	138	D17	-732.5	-243
37	TPO[5]	-9317.5	-243	88	AGNDH	-4982.5	-243	139	D16	-647.5	-243
38	TPO[5]	-9232.5	-243	89	SHIELDING	-4897.5	-243	140	DASHD	-562.5	-243
39	DIMI	-9147.5	-243	90	V1	-4812.5	-243	141	D15	-477.5	-243
40	DIMI	-9062.5	-243	91	V1	-4727.5	-243	142	D14	-392.5	-243
41	NBW	-8977.5	-243	92	V2	-4642.5	-243	143	DASHD	-307.5	-243
42	NBW	-8892.5	-243	93	V2	-4557.5	-243	144	D13	-222.5	-243
43	PINCTL	-8807.5	-243	94	V3	-4472.5	-243	145	D12	-137.5	-243
44	PINCTL	-8722.5	-243	95	V3	-4387.5	-243	146	DASHD	-52.5	-243
45	SHIELDING	-8637.5	-243	96	V4	-4302.5	-243	147	D11	32.5	-243
46	DIMO	-8552.5	-243	97	V4	-4217.5	-243	148	D10	117.5	-243
47	DIMO	-8467.5	-243	98	V5	-4132.5	-243	149	DASHD	202.5	-243
48	SHIELDING	-8382.5	-243	99	V5	-4047.5	-243	150	D07	287.5	-243
49	DITHER	-8297.5	-243	100	V6	-3962.5	-243	151	D06	372.5	-243
50	DITHER	-8212.5	-243	101	V6	-3877.5	-243	152	DASHD	457.5	-243
51	HFRC	-8127.5	-243	102	V7	-3792.5	-243	153	D05	542.5	-243

Pad	Name	X	Y	Pad	Name	X	Y	Pad	Name	X	Y
154	D04	627.5	-243	205	MASLOC	4962.5	-243	256	GND	9297.5	-243
155	DASHD	712.5	-243	206	CABC_EN[0]	5047.5	-243	257	SHIELDING	9382.5	-243
156	D03	797.5	-243	207	CABC_EN[0]	5132.5	-243	258	AVDDL	9467.5	-243
157	D02	882.5	-243	208	CABC_EN[1]	5217.5	-243	259	AVDDL	9552.5	-243
158	DASHD	967.5	-243	209	CABC_EN[1]	5302.5	-243	260	AVDDL	9637.5	-243
159	D01	1052.5	-243	210	OPDRV	5387.5	-243	261	AVDDL	9722.5	-243
160	D00	1137.5	-243	211	OPDRV	5472.5	-243	262	SHIELDING	9807.5	-243
161	DASHD	1222.5	-243	212	MODE	5557.5	-243	263	AGNDH	9892.5	-243
162	SHIELDING	1307.5	-243	213	MODE	5642.5	-243	264	AGNDH	9977.5	-243
163	GAML	1392.5	-243	214	IFSEL	5727.5	-243	265	AGNDH	10062.5	-243
164	GAML	1477.5	-243	215	IFSEL	5812.5	-243	266	AGNDH	10147.5	-243
165	V8	1562.5	-243	216	BIST	5897.5	-243	267	VREF_PAD	10232.5	-243
166	V8	1647.5	-243	217	BIST	5982.5	-243	268	VREF_PAD	10317.5	-243
167	V9	1732.5	-243	218	RES[0]	6067.5	-243	269	VCOMI	10402.5	-243
168	V9	1817.5	-243	219	RES[0]	6152.5	-243	270	VCOMI	10487.5	-243
169	V10	1902.5	-243	220	RES[1]	6237.5	-243	271	PWR_EN	10572.5	-243
170	V10	1987.5	-243	221	RES[1]	6322.5	-243	272	PWR_EN	10657.5	-243
171	V11	2072.5	-243	222	DCLKPOL	6407.5	-243	273	FBL	10742.5	-243
172	V11	2157.5	-243	223	DCLKPOL	6492.5	-243	274	FBL	10827.5	-243
173	V12	2242.5	-243	224	STBYB	6577.5	-243	275	FBH	10912.5	-243
174	V12	2327.5	-243	225	STBYB	6662.5	-243	276	FBH	10997.5	-243
175	V13	2412.5	-243	226	GRB	6747.5	-243	277	FBA	11082.5	-243
176	V13	2497.5	-243	227	GRB	6832.5	-243	278	FBA	11167.5	-243
177	V14	2582.5	-243	228	SHLR	6917.5	-243	279	AVDDG	11252.5	-243
178	V14	2667.5	-243	229	SHLR	7002.5	-243	280	AVDDG	11337.5	-243
179	SHIELDING	2752.5	-243	230	UPDN	7087.5	-243	281	DRVA	11422.5	-243
180	AGND	2837.5	-243	231	UPDN	7172.5	-243	282	DRVA	11507.5	-243
181	AGND	2922.5	-243	232	RES[2]	7257.5	-243	283	DRVH	11592.5	-243
182	AGND	3007.5	-243	233	RES[2]	7342.5	-243	284	DRVH	11677.5	-243
183	AGND	3092.5	-243	234	TPI[3]	7427.5	-243	285	DRVL	11762.5	-243
184	SHIELDING	3177.5	-243	235	TPI[3]	7512.5	-243	286	DRVL	11847.5	-243
185	AVDD	3262.5	-243	236	TPI[2]	7597.5	-243	287	DRVL_B	11932.5	-243
186	AVDD	3347.5	-243	237	TPI[2]	7682.5	-243	288	DRVL_B	12017.5	-243
187	AVDD	3432.5	-243	238	TPI[1]	7767.5	-243	289	VCOMO	12102.5	-243
188	AVDD	3517.5	-243	239	TPI[1]	7852.5	-243	290	VCOMO	12187.5	-243
189	SHIELDING	3602.5	-243	240	TPO[4]	7937.5	-243	291	COM2_IN	12272.5	-243
190	GND	3687.5	-243	241	TPO[4]	8022.5	-243	292	COM2_IN	12357.5	-243
191	GND	3772.5	-243	242	TPO[3]	8107.5	-243	293	STBNL	12303	-82
192	GND	3857.5	-243	243	TPO[3]	8192.5	-243	294	F_CTRLL	12403	-42
193	GND	3942.5	-243	244	TPO[2]	8277.5	-243	295	STV2L	12303	-2
194	SHIELDING	4027.5	-243	245	TPO[2]	8362.5	-243	296	STV1L	12403	38
195	VDD	4112.5	-243	246	TPO[1]	8447.5	-243	297	CKVL	12303	78
196	VDD	4197.5	-243	247	TPO[1]	8532.5	-243	298	UDL	12403	118
197	VDD	4282.5	-243	248	VDD	8617.5	-243	299	SYNC2L	12303	158
198	VDD	4367.5	-243	249	VDD	8702.5	-243	300	SYNC1L	12403	198
199	SHIELDING	4452.5	-243	250	VDD	8787.5	-243	301	OEVL	12303	238
200	DUAL	4537.5	-243	251	VDD	8872.5	-243	302	F_CTRLL	12403	278
201	DUAL	4622.5	-243	252	SHIELDING	8957.5	-243	303	SHIELDING	12203.04	258
202	MASL	4707.5	-243	253	GND	9042.5	-243	304	COM2_OUT	12153.04	258
203	MASL	4792.5	-243	254	GND	9127.5	-243	305	COM2_OUT	12103.04	258
204	MASLOC	4877.5	-243	255	GND	9212.5	-243	306	SHIELDING	12053.04	258

Pad	Name	X	Y	Pad	Name	X	Y	Pad	Name	X	Y
307	SO[1]	12010.58	113	358	SO[52]	11245.7	243	409	SO[103]	10480.83	113
308	SO[2]	11995.58	243	359	SO[53]	11230.71	113	410	SO[104]	10465.83	243
309	SO[3]	11980.58	113	360	SO[54]	11215.71	243	411	SO[105]	10450.84	113
310	SO[4]	11965.58	243	361	SO[55]	11200.71	113	412	SO[106]	10435.84	243
311	SO[5]	11950.59	113	362	SO[56]	11185.71	243	413	SO[107]	10420.84	113
312	SO[6]	11935.59	243	363	SO[57]	11170.72	113	414	SO[108]	10405.84	243
313	SO[7]	11920.59	113	364	SO[58]	11155.72	243	415	SO[109]	10390.85	113
314	SO[8]	11905.59	243	365	SO[59]	11140.72	113	416	SO[110]	10375.85	243
315	SO[9]	11890.6	113	366	SO[60]	11125.72	243	417	SO[111]	10360.85	113
316	SO[10]	11875.6	243	367	SO[61]	11110.73	113	418	SO[112]	10345.85	243
317	SO[11]	11860.6	113	368	SO[62]	11095.73	243	419	SO[113]	10330.86	113
318	SO[12]	11845.6	243	369	SO[63]	11080.73	113	420	SO[114]	10315.86	243
319	SO[13]	11830.61	113	370	SO[64]	11065.73	243	421	SO[115]	10300.86	113
320	SO[14]	11815.61	243	371	SO[65]	11050.74	113	422	SO[116]	10285.86	243
321	SO[15]	11800.61	113	372	SO[66]	11035.74	243	423	SO[117]	10270.87	113
322	SO[16]	11785.61	243	373	SO[67]	11020.74	113	424	SO[118]	10255.87	243
323	SO[17]	11770.62	113	374	SO[68]	11005.74	243	425	SO[119]	10240.87	113
324	SO[18]	11755.62	243	375	SO[69]	10990.75	113	426	SO[120]	10225.87	243
325	SO[19]	11740.62	113	376	SO[70]	10975.75	243	427	SO[121]	10210.88	113
326	SO[20]	11725.62	243	377	SO[71]	10960.75	113	428	SO[122]	10195.88	243
327	SO[21]	11710.63	113	378	SO[72]	10945.75	243	429	SO[123]	10180.88	113
328	SO[22]	11695.63	243	379	SO[73]	10930.76	113	430	SO[124]	10165.88	243
329	SO[23]	11680.63	113	380	SO[74]	10915.76	243	431	SO[125]	10150.89	113
330	SO[24]	11665.63	243	381	SO[75]	10900.76	113	432	SO[126]	10135.89	243
331	SO[25]	11650.64	113	382	SO[76]	10885.76	243	433	SO[127]	10120.89	113
332	SO[26]	11635.64	243	383	SO[77]	10870.77	113	434	SO[128]	10105.89	243
333	SO[27]	11620.64	113	384	SO[78]	10855.77	243	435	SO[129]	10090.9	113
334	SO[28]	11605.64	243	385	SO[79]	10840.77	113	436	SO[130]	10075.9	243
335	SO[29]	11590.65	113	386	SO[80]	10825.77	243	437	SO[131]	10060.9	113
336	SO[30]	11575.65	243	387	SO[81]	10810.78	113	438	SO[132]	10045.9	243
337	SO[31]	11560.65	113	388	SO[82]	10795.78	243	439	SO[133]	10030.91	113
338	SO[32]	11545.65	243	389	SO[83]	10780.78	113	440	SO[134]	10015.91	243
339	SO[33]	11530.66	113	390	SO[84]	10765.78	243	441	SO[135]	10000.91	113
340	SO[34]	11515.66	243	391	SO[85]	10750.79	113	442	SO[136]	9985.91	243
341	SO[35]	11500.66	113	392	SO[86]	10735.79	243	443	SO[137]	9970.92	113
342	SO[36]	11485.66	243	393	SO[87]	10720.79	113	444	SO[138]	9955.92	243
343	SO[37]	11470.67	113	394	SO[88]	10705.79	243	445	SO[139]	9940.92	113
344	SO[38]	11455.67	243	395	SO[89]	10690.8	113	446	SO[140]	9925.92	243
345	SO[39]	11440.67	113	396	SO[90]	10675.8	243	447	SO[141]	9910.93	113
346	SO[40]	11425.67	243	397	SO[91]	10660.8	113	448	SO[142]	9895.93	243
347	SO[41]	11410.68	113	398	SO[92]	10645.8	243	449	SO[143]	9880.93	113
348	SO[42]	11395.68	243	399	SO[93]	10630.81	113	450	SO[144]	9865.93	243
349	SO[43]	11380.68	113	400	SO[94]	10615.81	243	451	SO[145]	9850.94	113
350	SO[44]	11365.68	243	401	SO[95]	10600.81	113	452	SO[146]	9835.94	243
351	SO[45]	11350.69	113	402	SO[96]	10585.81	243	453	SO[147]	9820.94	113
352	SO[46]	11335.69	243	403	SO[97]	10570.82	113	454	SO[148]	9805.94	243
353	SO[47]	11320.69	113	404	SO[98]	10555.82	243	455	SO[149]	9790.95	113
354	SO[48]	11305.69	243	405	SO[99]	10540.82	113	456	SO[150]	9775.95	243
355	SO[49]	11290.7	113	406	SO[100]	10525.82	243	457	SO[151]	9760.95	113
356	SO[50]	11275.7	243	407	SO[101]	10510.83	113	458	SO[152]	9745.95	243
357	SO[51]	11260.7	113	408	SO[102]	10495.83	243	459	SO[153]	9730.96	113

Pad	Name	X	Y	Pad	Name	X	Y	Pad	Name	X	Y
460	SO[154]	9715.96	243	511	SO[205]	8951.09	113	562	SO[256]	8186.21	243
461	SO[155]	9700.96	113	512	SO[206]	8936.09	243	563	SO[257]	8171.22	113
462	SO[156]	9685.96	243	513	SO[207]	8921.09	113	564	SO[258]	8156.22	243
463	SO[157]	9670.97	113	514	SO[208]	8906.09	243	565	SO[259]	8141.22	113
464	SO[158]	9655.97	243	515	SO[209]	8891.1	113	566	SO[260]	8126.22	243
465	SO[159]	9640.97	113	516	SO[210]	8876.1	243	567	SO[261]	8111.23	113
466	SO[160]	9625.97	243	517	SO[211]	8861.1	113	568	SO[262]	8096.23	243
467	SO[161]	9610.98	113	518	SO[212]	8846.1	243	569	SO[263]	8081.23	113
468	SO[162]	9595.98	243	519	SO[213]	8831.11	113	570	SO[264]	8066.23	243
469	SO[163]	9580.98	113	520	SO[214]	8816.11	243	571	SO[265]	8051.24	113
470	SO[164]	9565.98	243	521	SO[215]	8801.11	113	572	SO[266]	8036.24	243
471	SO[165]	9550.99	113	522	SO[216]	8786.11	243	573	SO[267]	8021.24	113
472	SO[166]	9535.99	243	523	SO[217]	8771.12	113	574	SO[268]	8006.24	243
473	SO[167]	9520.99	113	524	SO[218]	8756.12	243	575	SO[269]	7991.25	113
474	SO[168]	9505.99	243	525	SO[219]	8741.12	113	576	SO[270]	7976.25	243
475	SO[169]	9491	113	526	SO[220]	8726.12	243	577	SO[271]	7961.25	113
476	SO[170]	9476	243	527	SO[221]	8711.13	113	578	SO[272]	7946.25	243
477	SO[171]	9461	113	528	SO[222]	8696.13	243	579	SO[273]	7931.26	113
478	SO[172]	9446	243	529	SO[223]	8681.13	113	580	SO[274]	7916.26	243
479	SO[173]	9431.01	113	530	SO[224]	8666.13	243	581	SO[275]	7901.26	113
480	SO[174]	9416.01	243	531	SO[225]	8651.14	113	582	SO[276]	7886.26	243
481	SO[175]	9401.01	113	532	SO[226]	8636.14	243	583	SO[277]	7871.27	113
482	SO[176]	9386.01	243	533	SO[227]	8621.14	113	584	SO[278]	7856.27	243
483	SO[177]	9371.02	113	534	SO[228]	8606.14	243	585	SO[279]	7841.27	113
484	SO[178]	9356.02	243	535	SO[229]	8591.15	113	586	SO[280]	7826.27	243
485	SO[179]	9341.02	113	536	SO[230]	8576.15	243	587	SO[281]	7811.28	113
486	SO[180]	9326.02	243	537	SO[231]	8561.15	113	588	SO[282]	7796.28	243
487	SO[181]	9311.03	113	538	SO[232]	8546.15	243	589	SO[283]	7781.28	113
488	SO[182]	9296.03	243	539	SO[233]	8531.16	113	590	SO[284]	7766.28	243
489	SO[183]	9281.03	113	540	SO[234]	8516.16	243	591	SO[285]	7751.29	113
490	SO[184]	9266.03	243	541	SO[235]	8501.16	113	592	SO[286]	7736.29	243
491	SO[185]	9251.04	113	542	SO[236]	8486.16	243	593	SO[287]	7721.29	113
492	SO[186]	9236.04	243	543	SO[237]	8471.17	113	594	SO[288]	7706.29	243
493	SO[187]	9221.04	113	544	SO[238]	8456.17	243	595	SO[289]	7691.3	113
494	SO[188]	9206.04	243	545	SO[239]	8441.17	113	596	SO[290]	7676.3	243
495	SO[189]	9191.05	113	546	SO[240]	8426.17	243	597	SO[291]	7661.3	113
496	SO[190]	9176.05	243	547	SO[241]	8411.18	113	598	SO[292]	7646.3	243
497	SO[191]	9161.05	113	548	SO[242]	8396.18	243	599	SO[293]	7631.31	113
498	SO[192]	9146.05	243	549	SO[243]	8381.18	113	600	SO[294]	7616.31	243
499	SO[193]	9131.06	113	550	SO[244]	8366.18	243	601	SO[295]	7601.31	113
500	SO[194]	9116.06	243	551	SO[245]	8351.19	113	602	SO[296]	7586.31	243
501	SO[195]	9101.06	113	552	SO[246]	8336.19	243	603	SO[297]	7571.32	113
502	SO[196]	9086.06	243	553	SO[247]	8321.19	113	604	SO[298]	7556.32	243
503	SO[197]	9071.07	113	554	SO[248]	8306.19	243	605	SO[299]	7541.32	113
504	SO[198]	9056.07	243	555	SO[249]	8291.2	113	606	SO[300]	7526.32	243
505	SO[199]	9041.07	113	556	SO[250]	8276.2	243	607	SO[301]	7511.33	113
506	SO[200]	9026.07	243	557	SO[251]	8261.2	113	608	SO[302]	7496.33	243
507	SO[201]	9011.08	113	558	SO[252]	8246.2	243	609	SO[303]	7481.33	113
508	SO[202]	8996.08	243	559	SO[253]	8231.21	113	610	SO[304]	7466.33	243
509	SO[203]	8981.08	113	560	SO[254]	8216.21	243	611	SO[305]	7451.34	113
510	SO[204]	8966.08	243	561	SO[255]	8201.21	113	612	SO[306]	7436.34	243

Pad	Name	X	Y	Pad	Name	X	Y	Pad	Name	X	Y
613	SO[307]	7421.34	113	664	SO[358]	6656.47	243	715	SO[409]	5891.6	113
614	SO[308]	7406.34	243	665	SO[359]	6641.47	113	716	SO[410]	5876.6	243
615	SO[309]	7391.35	113	666	SO[360]	6626.47	243	717	SO[411]	5861.6	113
616	SO[310]	7376.35	243	667	SO[361]	6611.48	113	718	SO[412]	5846.6	243
617	SO[311]	7361.35	113	668	SO[362]	6596.48	243	719	SO[413]	5831.61	113
618	SO[312]	7346.35	243	669	SO[363]	6581.48	113	720	SO[414]	5816.61	243
619	SO[313]	7331.36	113	670	SO[364]	6566.48	243	721	SO[415]	5801.61	113
620	SO[314]	7316.36	243	671	SO[365]	6551.49	113	722	SO[416]	5786.61	243
621	SO[315]	7301.36	113	672	SO[366]	6536.49	243	723	SO[417]	5771.62	113
622	SO[316]	7286.36	243	673	SO[367]	6521.49	113	724	SO[418]	5756.62	243
623	SO[317]	7271.37	113	674	SO[368]	6506.49	243	725	SO[419]	5741.62	113
624	SO[318]	7256.37	243	675	SO[369]	6491.5	113	726	SO[420]	5726.62	243
625	SO[319]	7241.37	113	676	SO[370]	6476.5	243	727	SO[421]	5711.63	113
626	SO[320]	7226.37	243	677	SO[371]	6461.5	113	728	SO[422]	5696.63	243
627	SO[321]	7211.38	113	678	SO[372]	6446.5	243	729	SO[423]	5681.63	113
628	SO[322]	7196.38	243	679	SO[373]	6431.51	113	730	SO[424]	5666.63	243
629	SO[323]	7181.38	113	680	SO[374]	6416.51	243	731	SO[425]	5651.64	113
630	SO[324]	7166.38	243	681	SO[375]	6401.51	113	732	SO[426]	5636.64	243
631	SO[325]	7151.39	113	682	SO[376]	6386.51	243	733	SO[427]	5621.64	113
632	SO[326]	7136.39	243	683	SO[377]	6371.52	113	734	SO[428]	5606.64	243
633	SO[327]	7121.39	113	684	SO[378]	6356.52	243	735	SO[429]	5591.65	113
634	SO[328]	7106.39	243	685	SO[379]	6341.52	113	736	SO[430]	5576.65	243
635	SO[329]	7091.4	113	686	SO[380]	6326.52	243	737	SO[431]	5561.65	113
636	SO[330]	7076.4	243	687	SO[381]	6311.53	113	738	SO[432]	5546.65	243
637	SO[331]	7061.4	113	688	SO[382]	6296.53	243	739	SO[433]	5531.66	113
638	SO[332]	7046.4	243	689	SO[383]	6281.53	113	740	SO[434]	5516.66	243
639	SO[333]	7031.41	113	690	SO[384]	6266.53	243	741	SO[435]	5501.66	113
640	SO[334]	7016.41	243	691	SO[385]	6251.54	113	742	SO[436]	5486.66	243
641	SO[335]	7001.41	113	692	SO[386]	6236.54	243	743	SO[437]	5471.67	113
642	SO[336]	6986.41	243	693	SO[387]	6221.54	113	744	SO[438]	5456.67	243
643	SO[337]	6971.42	113	694	SO[388]	6206.54	243	745	SO[439]	5441.67	113
644	SO[338]	6956.42	243	695	SO[389]	6191.55	113	746	SO[440]	5426.67	243
645	SO[339]	6941.42	113	696	SO[390]	6176.55	243	747	SO[441]	5411.68	113
646	SO[340]	6926.42	243	697	SO[391]	6161.55	113	748	SO[442]	5396.68	243
647	SO[341]	6911.43	113	698	SO[392]	6146.55	243	749	SO[443]	5381.68	113
648	SO[342]	6896.43	243	699	SO[393]	6131.56	113	750	SO[444]	5366.68	243
649	SO[343]	6881.43	113	700	SO[394]	6116.56	243	751	SO[445]	5351.69	113
650	SO[344]	6866.43	243	701	SO[395]	6101.56	113	752	SO[446]	5336.69	243
651	SO[345]	6851.44	113	702	SO[396]	6086.56	243	753	SO[447]	5321.69	113
652	SO[346]	6836.44	243	703	SO[397]	6071.57	113	754	SO[448]	5306.69	243
653	SO[347]	6821.44	113	704	SO[398]	6056.57	243	755	SO[449]	5291.7	113
654	SO[348]	6806.44	243	705	SO[399]	6041.57	113	756	SO[450]	5276.7	243
655	SO[349]	6791.45	113	706	SO[400]	6026.57	243	757	SO[451]	5261.7	113
656	SO[350]	6776.45	243	707	SO[401]	6011.58	113	758	SO[452]	5246.7	243
657	SO[351]	6761.45	113	708	SO[402]	5996.58	243	759	SO[453]	5231.71	113
658	SO[352]	6746.45	243	709	SO[403]	5981.58	113	760	SO[454]	5216.71	243
659	SO[353]	6731.46	113	710	SO[404]	5966.58	243	761	SO[455]	5201.71	113
660	SO[354]	6716.46	243	711	SO[405]	5951.59	113	762	SO[456]	5186.71	243
661	SO[355]	6701.46	113	712	SO[406]	5936.59	243	763	SO[457]	5171.72	113
662	SO[356]	6686.46	243	713	SO[407]	5921.59	113	764	SO[458]	5156.72	243
663	SO[357]	6671.47	113	714	SO[408]	5906.59	243	765	SO[459]	5141.72	113

Pad	Name	X	Y	Pad	Name	X	Y	Pad	Name	X	Y
766	SO[460]	5126.72	243	817	SO[511]	4361.85	113	868	SO[562]	3596.98	243
767	SO[461]	5111.73	113	818	SO[512]	4346.85	243	869	SO[563]	3581.98	113
768	SO[462]	5096.73	243	819	SO[513]	4331.86	113	870	SO[564]	3566.98	243
769	SO[463]	5081.73	113	820	SO[514]	4316.86	243	871	SO[565]	3551.99	113
770	SO[464]	5066.73	243	821	SO[515]	4301.86	113	872	SO[566]	3536.99	243
771	SO[465]	5051.74	113	822	SO[516]	4286.86	243	873	SO[567]	3521.99	113
772	SO[466]	5036.74	243	823	SO[517]	4271.87	113	874	SO[568]	3506.99	243
773	SO[467]	5021.74	113	824	SO[518]	4256.87	243	875	SO[569]	3492	113
774	SO[468]	5006.74	243	825	SO[519]	4241.87	113	876	SO[570]	3477	243
775	SO[469]	4991.75	113	826	SO[520]	4226.87	243	877	SO[571]	3462	113
776	SO[470]	4976.75	243	827	SO[521]	4211.88	113	878	SO[572]	3447	243
777	SO[471]	4961.75	113	828	SO[522]	4196.88	243	879	SO[573]	3432.01	113
778	SO[472]	4946.75	243	829	SO[523]	4181.88	113	880	SO[574]	3417.01	243
779	SO[473]	4931.76	113	830	SO[524]	4166.88	243	881	SO[575]	3402.01	113
780	SO[474]	4916.76	243	831	SO[525]	4151.89	113	882	SO[576]	3387.01	243
781	SO[475]	4901.76	113	832	SO[526]	4136.89	243	883	SO[577]	3372.02	113
782	SO[476]	4886.76	243	833	SO[527]	4121.89	113	884	SO[578]	3357.02	243
783	SO[477]	4871.77	113	834	SO[528]	4106.89	243	885	SO[579]	3342.02	113
784	SO[478]	4856.77	243	835	SO[529]	4091.9	113	886	SO[580]	3327.02	243
785	SO[479]	4841.77	113	836	SO[530]	4076.9	243	887	SO[581]	3312.03	113
786	SO[480]	4826.77	243	837	SO[531]	4061.9	113	888	SO[582]	3297.03	243
787	SO[481]	4811.78	113	838	SO[532]	4046.9	243	889	SO[583]	3282.03	113
788	SO[482]	4796.78	243	839	SO[533]	4031.91	113	890	SO[584]	3267.03	243
789	SO[483]	4781.78	113	840	SO[534]	4016.91	243	891	SO[585]	3252.04	113
790	SO[484]	4766.78	243	841	SO[535]	4001.91	113	892	SO[586]	3237.04	243
791	SO[485]	4751.79	113	842	SO[536]	3986.91	243	893	SO[587]	3222.04	113
792	SO[486]	4736.79	243	843	SO[537]	3971.92	113	894	SO[588]	3207.04	243
793	SO[487]	4721.79	113	844	SO[538]	3956.92	243	895	SO[589]	3192.05	113
794	SO[488]	4706.79	243	845	SO[539]	3941.92	113	896	SO[590]	3177.05	243
795	SO[489]	4691.8	113	846	SO[540]	3926.92	243	897	SO[591]	3162.05	113
796	SO[490]	4676.8	243	847	SO[541]	3911.93	113	898	SO[592]	3147.05	243
797	SO[491]	4661.8	113	848	SO[542]	3896.93	243	899	SO[593]	3132.06	113
798	SO[492]	4646.8	243	849	SO[543]	3881.93	113	900	SO[594]	3117.06	243
799	SO[493]	4631.81	113	850	SO[544]	3866.93	243	901	SO[595]	3102.06	113
800	SO[494]	4616.81	243	851	SO[545]	3851.94	113	902	SO[596]	3087.06	243
801	SO[495]	4601.81	113	852	SO[546]	3836.94	243	903	SO[597]	3072.07	113
802	SO[496]	4586.81	243	853	SO[547]	3821.94	113	904	SO[598]	3057.07	243
803	SO[497]	4571.82	113	854	SO[548]	3806.94	243	905	SO[599]	3042.07	113
804	SO[498]	4556.82	243	855	SO[549]	3791.95	113	906	SO[600]	3027.07	243
805	SO[499]	4541.82	113	856	SO[550]	3776.95	243	907	SO[601]	3012.08	113
806	SO[500]	4526.82	243	857	SO[551]	3761.95	113	908	SO[602]	2997.08	243
807	SO[501]	4511.83	113	858	SO[552]	3746.95	243	909	SO[603]	2982.08	113
808	SO[502]	4496.83	243	859	SO[553]	3731.96	113	910	SO[604]	2967.08	243
809	SO[503]	4481.83	113	860	SO[554]	3716.96	243	911	SO[605]	2952.09	113
810	SO[504]	4466.83	243	861	SO[555]	3701.96	113	912	SO[606]	2937.09	243
811	SO[505]	4451.84	113	862	SO[556]	3686.96	243	913	SO[607]	2922.09	113
812	SO[506]	4436.84	243	863	SO[557]	3671.97	113	914	SO[608]	2907.09	243
813	SO[507]	4421.84	113	864	SO[558]	3656.97	243	915	SO[609]	2892.1	113
814	SO[508]	4406.84	243	865	SO[559]	3641.97	113	916	SO[610]	2877.1	243
815	SO[509]	4391.85	113	866	SO[560]	3626.97	243	917	SO[611]	2862.1	113
816	SO[510]	4376.85	243	867	SO[561]	3611.98	113	918	SO[612]	2847.1	243

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919	SO[613]	2832.11	113	970	SO[664]	2067.23	243	1021	SO[715]	1302.36	113
920	SO[614]	2817.11	243	971	SO[665]	2052.24	113	1022	SO[716]	1287.36	243
921	SO[615]	2802.11	113	972	SO[666]	2037.24	243	1023	SO[717]	1272.37	113
922	SO[616]	2787.11	243	973	SO[667]	2022.24	113	1024	SO[718]	1257.37	243
923	SO[617]	2772.12	113	974	SO[668]	2007.24	243	1025	SO[719]	1242.37	113
924	SO[618]	2757.12	243	975	SO[669]	1992.25	113	1026	SO[720]	1227.37	243
925	SO[619]	2742.12	113	976	SO[670]	1977.25	243	1027	SO[721]	1212.38	113
926	SO[620]	2727.12	243	977	SO[671]	1962.25	113	1028	SO[722]	1197.38	243
927	SO[621]	2712.13	113	978	SO[672]	1947.25	243	1029	SO[723]	1182.38	113
928	SO[622]	2697.13	243	979	SO[673]	1932.26	113	1030	SO[724]	1167.38	243
929	SO[623]	2682.13	113	980	SO[674]	1917.26	243	1031	SO[725]	1152.39	113
930	SO[624]	2667.13	243	981	SO[675]	1902.26	113	1032	SO[726]	1137.39	243
931	SO[625]	2652.14	113	982	SO[676]	1887.26	243	1033	SO[727]	1122.39	113
932	SO[626]	2637.14	243	983	SO[677]	1872.27	113	1034	SO[728]	1107.39	243
933	SO[627]	2622.14	113	984	SO[678]	1857.27	243	1035	SO[729]	1092.4	113
934	SO[628]	2607.14	243	985	SO[679]	1842.27	113	1036	SO[730]	1077.4	243
935	SO[629]	2592.15	113	986	SO[680]	1827.27	243	1037	SO[731]	1062.4	113
936	SO[630]	2577.15	243	987	SO[681]	1812.28	113	1038	SO[732]	1047.4	243
937	SO[631]	2562.15	113	988	SO[682]	1797.28	243	1039	SO[733]	1032.41	113
938	SO[632]	2547.15	243	989	SO[683]	1782.28	113	1040	SO[734]	1017.41	243
939	SO[633]	2532.16	113	990	SO[684]	1767.28	243	1041	SO[735]	1002.41	113
940	SO[634]	2517.16	243	991	SO[685]	1752.29	113	1042	SO[736]	987.41	243
941	SO[635]	2502.16	113	992	SO[686]	1737.29	243	1043	SO[737]	972.42	113
942	SO[636]	2487.16	243	993	SO[687]	1722.29	113	1044	SO[738]	957.42	243
943	SO[637]	2472.17	113	994	SO[688]	1707.29	243	1045	SO[739]	942.42	113
944	SO[638]	2457.17	243	995	SO[689]	1692.3	113	1046	SO[740]	927.42	243
945	SO[639]	2442.17	113	996	SO[690]	1677.3	243	1047	SO[741]	912.43	113
946	SO[640]	2427.17	243	997	SO[691]	1662.3	113	1048	SO[742]	897.43	243
947	SO[641]	2412.18	113	998	SO[692]	1647.3	243	1049	SO[743]	882.43	113
948	SO[642]	2397.18	243	999	SO[693]	1632.31	113	1050	SO[744]	867.43	243
949	SO[643]	2382.18	113	1000	SO[694]	1617.31	243	1051	SO[745]	852.44	113
950	SO[644]	2367.18	243	1001	SO[695]	1602.31	113	1052	SO[746]	837.44	243
951	SO[645]	2352.19	113	1002	SO[696]	1587.31	243	1053	SO[747]	822.44	113
952	SO[646]	2337.19	243	1003	SO[697]	1572.32	113	1054	SO[748]	807.44	243
953	SO[647]	2322.19	113	1004	SO[698]	1557.32	243	1055	SO[749]	792.45	113
954	SO[648]	2307.19	243	1005	SO[699]	1542.32	113	1056	SO[750]	777.45	243
955	SO[649]	2292.2	113	1006	SO[700]	1527.32	243	1057	SO[751]	762.45	113
956	SO[650]	2277.2	243	1007	SO[701]	1512.33	113	1058	SO[752]	747.45	243
957	SO[651]	2262.2	113	1008	SO[702]	1497.33	243	1059	SO[753]	732.46	113
958	SO[652]	2247.2	243	1009	SO[703]	1482.33	113	1060	SO[754]	717.46	243
959	SO[653]	2232.21	113	1010	SO[704]	1467.33	243	1061	SO[755]	702.46	113
960	SO[654]	2217.21	243	1011	SO[705]	1452.34	113	1062	SO[756]	687.46	243
961	SO[655]	2202.21	113	1012	SO[706]	1437.34	243	1063	SO[757]	672.47	113
962	SO[656]	2187.21	243	1013	SO[707]	1422.34	113	1064	SO[758]	657.47	243
963	SO[657]	2172.22	113	1014	SO[708]	1407.34	243	1065	SO[759]	642.47	113
964	SO[658]	2157.22	243	1015	SO[709]	1392.35	113	1066	SO[760]	627.47	243
965	SO[659]	2142.22	113	1016	SO[710]	1377.35	243	1067	SO[761]	612.48	113
966	SO[660]	2127.22	243	1017	SO[711]	1362.35	113	1068	SO[762]	597.48	243
967	SO[661]	2112.23	113	1018	SO[712]	1347.35	243	1069	SO[763]	582.48	113
968	SO[662]	2097.23	243	1019	SO[713]	1332.36	113	1070	SO[764]	567.48	243
969	SO[663]	2082.23	113	1020	SO[714]	1317.36	243	1071	SO[765]	552.49	113

Pad	Name	X	Y	Pad	Name	X	Y	Pad	Name	X	Y
1072	SO[766]	537.49	243	1123	SO[808]	-1092.4	113	1174	SO[859]	-1857.27	243
1073	SO[767]	522.49	113	1124	SO[809]	-1107.39	243	1175	SO[860]	-1872.27	113
1074	SO[768]	507.49	243	1125	SO[810]	-1122.39	113	1176	SO[861]	-1887.26	243
1075	SHIELDING	455	258	1126	SO[811]	-1137.39	243	1177	SO[862]	-1902.26	113
1076	SHIELDING	405	258	1127	SO[812]	-1152.39	113	1178	SO[863]	-1917.26	243
1077	SHIELDING	355	258	1128	SO[813]	-1167.38	243	1179	SO[864]	-1932.26	113
1078	SHIELDING	50	258	1129	SO[814]	-1182.38	113	1180	SO[865]	-1947.25	243
1079	SHIELDING	0	258	1130	SO[815]	-1197.38	243	1181	SO[866]	-1962.25	113
1080	SHIELDING	-50	258	1131	SO[816]	-1212.38	113	1182	SO[867]	-1977.25	243
1081	SHIELDING	-355	258	1132	SO[817]	-1227.37	243	1183	SO[868]	-1992.25	113
1082	SHIELDING	-405	258	1133	SO[818]	-1242.37	113	1184	SO[869]	-2007.24	243
1083	SHIELDING	-455	258	1134	SO[819]	-1257.37	243	1185	SO[870]	-2022.24	113
1084	SO[769]	-507.49	243	1135	SO[820]	-1272.37	113	1186	SO[871]	-2037.24	243
1085	SO[770]	-522.49	113	1136	SO[821]	-1287.36	243	1187	SO[872]	-2052.24	113
1086	SO[771]	-537.49	243	1137	SO[822]	-1302.36	113	1188	SO[873]	-2067.23	243
1087	SO[772]	-552.49	113	1138	SO[823]	-1317.36	243	1189	SO[874]	-2082.23	113
1088	SO[773]	-567.48	243	1139	SO[824]	-1332.36	113	1190	SO[875]	-2097.23	243
1089	SO[774]	-582.48	113	1140	SO[825]	-1347.35	243	1191	SO[876]	-2112.23	113
1090	SO[775]	-597.48	243	1141	SO[826]	-1362.35	113	1192	SO[877]	-2127.22	243
1091	SO[776]	-612.48	113	1142	SO[827]	-1377.35	243	1193	SO[878]	-2142.22	113
1092	SO[777]	-627.47	243	1143	SO[828]	-1392.35	113	1194	SO[879]	-2157.22	243
1093	SO[778]	-642.47	113	1144	SO[829]	-1407.34	243	1195	SO[880]	-2172.22	113
1094	SO[779]	-657.47	243	1145	SO[830]	-1422.34	113	1196	SO[881]	-2187.21	243
1095	SO[780]	-672.47	113	1146	SO[831]	-1437.34	243	1197	SO[882]	-2202.21	113
1096	SO[781]	-687.46	243	1147	SO[832]	-1452.34	113	1198	SO[883]	-2217.21	243
1097	SO[782]	-702.46	113	1148	SO[833]	-1467.33	243	1199	SO[884]	-2232.21	113
1098	SO[783]	-717.46	243	1149	SO[834]	-1482.33	113	1200	SO[885]	-2247.2	243
1099	SO[784]	-732.46	113	1150	SO[835]	-1497.33	243	1201	SO[886]	-2262.2	113
1100	SO[785]	-747.45	243	1151	SO[836]	-1512.33	113	1202	SO[887]	-2277.2	243
1101	SO[786]	-762.45	113	1152	SO[837]	-1527.32	243	1203	SO[888]	-2292.2	113
1102	SO[787]	-777.45	243	1153	SO[838]	-1542.32	113	1204	SO[889]	-2307.19	243
1103	SO[788]	-792.45	113	1154	SO[839]	-1557.32	243	1205	SO[890]	-2322.19	113
1104	SO[789]	-807.44	243	1155	SO[840]	-1572.32	113	1206	SO[891]	-2337.19	243
1105	SO[790]	-822.44	113	1156	SO[841]	-1587.31	243	1207	SO[892]	-2352.19	113
1106	SO[791]	-837.44	243	1157	SO[842]	-1602.31	113	1208	SO[893]	-2367.18	243
1107	SO[792]	-852.44	113	1158	SO[843]	-1617.31	243	1209	SO[894]	-2382.18	113
1108	SO[793]	-867.43	243	1159	SO[844]	-1632.31	113	1210	SO[895]	-2397.18	243
1109	SO[794]	-882.43	113	1160	SO[845]	-1647.3	243	1211	SO[896]	-2412.18	113
1110	SO[795]	-897.43	243	1161	SO[846]	-1662.3	113	1212	SO[897]	-2427.17	243
1111	SO[796]	-912.43	113	1162	SO[847]	-1677.3	243	1213	SO[898]	-2442.17	113
1112	SO[797]	-927.42	243	1163	SO[848]	-1692.3	113	1214	SO[899]	-2457.17	243
1113	SO[798]	-942.42	113	1164	SO[849]	-1707.29	243	1215	SO[900]	-2472.17	113
1114	SO[799]	-957.42	243	1165	SO[850]	-1722.29	113	1216	SO[901]	-2487.16	243
1115	SO[800]	-972.42	113	1166	SO[851]	-1737.29	243	1217	SO[902]	-2502.16	113
1116	SO[801]	-987.41	243	1167	SO[852]	-1752.29	113	1218	SO[903]	-2517.16	243
1117	SO[802]	-1002.41	113	1168	SO[853]	-1767.28	243	1219	SO[904]	-2532.16	113
1118	SO[803]	-1017.41	243	1169	SO[854]	-1782.28	113	1220	SO[905]	-2547.15	243
1119	SO[804]	-1032.41	113	1170	SO[855]	-1797.28	243	1221	SO[906]	-2562.15	113
1120	SO[805]	-1047.4	243	1171	SO[856]	-1812.28	113	1222	SO[907]	-2577.15	243
1121	SO[806]	-1062.4	113	1172	SO[857]	-1827.27	243	1223	SO[908]	-2592.15	113
1122	SO[807]	-1077.4	243	1173	SO[858]	-1842.27	113	1224	SO[909]	-2607.14	243

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1225	SO[910]	-2622.14	113	1276	SO[961]	-3387.01	243	1327	SO[1012]	-4151.89	113
1226	SO[911]	-2637.14	243	1277	SO[962]	-3402.01	113	1328	SO[1013]	-4166.88	243
1227	SO[912]	-2652.14	113	1278	SO[963]	-3417.01	243	1329	SO[1014]	-4181.88	113
1228	SO[913]	-2667.13	243	1279	SO[964]	-3432.01	113	1330	SO[1015]	-4196.88	243
1229	SO[914]	-2682.13	113	1280	SO[965]	-3447	243	1331	SO[1016]	-4211.88	113
1230	SO[915]	-2697.13	243	1281	SO[966]	-3462	113	1332	SO[1017]	-4226.87	243
1231	SO[916]	-2712.13	113	1282	SO[967]	-3477	243	1333	SO[1018]	-4241.87	113
1232	SO[917]	-2727.12	243	1283	SO[968]	-3492	113	1334	SO[1019]	-4256.87	243
1233	SO[918]	-2742.12	113	1284	SO[969]	-3506.99	243	1335	SO[1020]	-4271.87	113
1234	SO[919]	-2757.12	243	1285	SO[970]	-3521.99	113	1336	SO[1021]	-4286.86	243
1235	SO[920]	-2772.12	113	1286	SO[971]	-3536.99	243	1337	SO[1022]	-4301.86	113
1236	SO[921]	-2787.11	243	1287	SO[972]	-3551.99	113	1338	SO[1023]	-4316.86	243
1237	SO[922]	-2802.11	113	1288	SO[973]	-3566.98	243	1339	SO[1024]	-4331.86	113
1238	SO[923]	-2817.11	243	1289	SO[974]	-3581.98	113	1340	SO[1025]	-4346.85	243
1239	SO[924]	-2832.11	113	1290	SO[975]	-3596.98	243	1341	SO[1026]	-4361.85	113
1240	SO[925]	-2847.1	243	1291	SO[976]	-3611.98	113	1342	SO[1027]	-4376.85	243
1241	SO[926]	-2862.1	113	1292	SO[977]	-3626.97	243	1343	SO[1028]	-4391.85	113
1242	SO[927]	-2877.1	243	1293	SO[978]	-3641.97	113	1344	SO[1029]	-4406.84	243
1243	SO[928]	-2892.1	113	1294	SO[979]	-3656.97	243	1345	SO[1030]	-4421.84	113
1244	SO[929]	-2907.09	243	1295	SO[980]	-3671.97	113	1346	SO[1031]	-4436.84	243
1245	SO[930]	-2922.09	113	1296	SO[981]	-3686.96	243	1347	SO[1032]	-4451.84	113
1246	SO[931]	-2937.09	243	1297	SO[982]	-3701.96	113	1348	SO[1033]	-4466.83	243
1247	SO[932]	-2952.09	113	1298	SO[983]	-3716.96	243	1349	SO[1034]	-4481.83	113
1248	SO[933]	-2967.08	243	1299	SO[984]	-3731.96	113	1350	SO[1035]	-4496.83	243
1249	SO[934]	-2982.08	113	1300	SO[985]	-3746.95	243	1351	SO[1036]	-4511.83	113
1250	SO[935]	-2997.08	243	1301	SO[986]	-3761.95	113	1352	SO[1037]	-4526.82	243
1251	SO[936]	-3012.08	113	1302	SO[987]	-3776.95	243	1353	SO[1038]	-4541.82	113
1252	SO[937]	-3027.07	243	1303	SO[988]	-3791.95	113	1354	SO[1039]	-4556.82	243
1253	SO[938]	-3042.07	113	1304	SO[989]	-3806.94	243	1355	SO[1040]	-4571.82	113
1254	SO[939]	-3057.07	243	1305	SO[990]	-3821.94	113	1356	SO[1041]	-4586.81	243
1255	SO[940]	-3072.07	113	1306	SO[991]	-3836.94	243	1357	SO[1042]	-4601.81	113
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1261	SO[946]	-3162.05	113	1312	SO[997]	-3926.92	243	1363	SO[1048]	-4691.8	113
1262	SO[947]	-3177.05	243	1313	SO[998]	-3941.92	113	1364	SO[1049]	-4706.79	243
1263	SO[948]	-3192.05	113	1314	SO[999]	-3956.92	243	1365	SO[1050]	-4721.79	113
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1266	SO[951]	-3237.04	243	1317	SO[1002]	-4001.91	113	1368	SO[1053]	-4766.78	243
1267	SO[952]	-3252.04	113	1318	SO[1003]	-4016.91	243	1369	SO[1054]	-4781.78	113
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1272	SO[957]	-3327.02	243	1323	SO[1008]	-4091.9	113	1374	SO[1059]	-4856.77	243
1273	SO[958]	-3342.02	113	1324	SO[1009]	-4106.89	243	1375	SO[1060]	-4871.77	113
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1380	SO[1065]	-4946.75	243	1431	SO[1116]	-5711.63	113	1482	SO[1167]	-6476.5	243
1381	SO[1066]	-4961.75	113	1432	SO[1117]	-5726.62	243	1483	SO[1168]	-6491.5	113
1382	SO[1067]	-4976.75	243	1433	SO[1118]	-5741.62	113	1484	SO[1169]	-6506.49	243
1383	SO[1068]	-4991.75	113	1434	SO[1119]	-5756.62	243	1485	SO[1170]	-6521.49	113
1384	SO[1069]	-5006.74	243	1435	SO[1120]	-5771.62	113	1486	SO[1171]	-6536.49	243
1385	SO[1070]	-5021.74	113	1436	SO[1121]	-5786.61	243	1487	SO[1172]	-6551.49	113
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1388	SO[1073]	-5066.73	243	1439	SO[1124]	-5831.61	113	1490	SO[1175]	-6596.48	243
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1398	SO[1083]	-5216.71	243	1449	SO[1134]	-5981.58	113	1500	SO[1185]	-6746.45	243
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1418	SO[1103]	-5516.66	243	1469	SO[1154]	-6281.53	113	1520	SO[1205]	-7046.4	243
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1428	SO[1113]	-5666.63	243	1479	SO[1164]	-6431.51	113	1530	SO[1215]	-7196.38	243

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1533	SO[1218]	-7241.37	113	1584	SO[1269]	-8006.24	243	1635	SO[1320]	-8771.12	113
1534	SO[1219]	-7256.37	243	1585	SO[1270]	-8021.24	113	1636	SO[1321]	-8786.11	243
1535	SO[1220]	-7271.37	113	1586	SO[1271]	-8036.24	243	1637	SO[1322]	-8801.11	113
1536	SO[1221]	-7286.36	243	1587	SO[1272]	-8051.24	113	1638	SO[1323]	-8816.11	243
1537	SO[1222]	-7301.36	113	1588	SO[1273]	-8066.23	243	1639	SO[1324]	-8831.11	113
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1685	SO[1370]	-9520.99	113	1736	SO[1421]	-10285.86	243	1787	SO[1472]	-11050.74	113
1686	SO[1371]	-9535.99	243	1737	SO[1422]	-10300.86	113	1788	SO[1473]	-11065.73	243
1687	SO[1372]	-9550.99	113	1738	SO[1423]	-10315.86	243	1789	SO[1474]	-11080.73	113
1688	SO[1373]	-9565.98	243	1739	SO[1424]	-10330.86	113	1790	SO[1475]	-11095.73	243
1689	SO[1374]	-9580.98	113	1740	SO[1425]	-10345.85	243	1791	SO[1476]	-11110.73	113
1690	SO[1375]	-9595.98	243	1741	SO[1426]	-10360.85	113	1792	SO[1477]	-11125.72	243
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1692	SO[1377]	-9625.97	243	1743	SO[1428]	-10390.85	113	1794	SO[1479]	-11155.72	243
1693	SO[1378]	-9640.97	113	1744	SO[1429]	-10405.84	243	1795	SO[1480]	-11170.72	113
1694	SO[1379]	-9655.97	243	1745	SO[1430]	-10420.84	113	1796	SO[1481]	-11185.71	243
1695	SO[1380]	-9670.97	113	1746	SO[1431]	-10435.84	243	1797	SO[1482]	-11200.71	113
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1714	SO[1399]	-9955.92	243	1765	SO[1450]	-10720.79	113	1816	SO[1501]	-11485.66	243
1715	SO[1400]	-9970.92	113	1766	SO[1451]	-10735.79	243	1817	SO[1502]	-11500.66	113
1716	SO[1401]	-9985.91	243	1767	SO[1452]	-10750.79	113	1818	SO[1503]	-11515.66	243
1717	SO[1402]	-10000.91	113	1768	SO[1453]	-10765.78	243	1819	SO[1504]	-11530.66	113
1718	SO[1403]	-10015.91	243	1769	SO[1454]	-10780.78	113	1820	SO[1505]	-11545.65	243
1719	SO[1404]	-10030.91	113	1770	SO[1455]	-10795.78	243	1821	SO[1506]	-11560.65	113
1720	SO[1405]	-10045.9	243	1771	SO[1456]	-10810.78	113	1822	SO[1507]	-11575.65	243
1721	SO[1406]	-10060.9	113	1772	SO[1457]	-10825.77	243	1823	SO[1508]	-11590.65	113
1722	SO[1407]	-10075.9	243	1773	SO[1458]	-10840.77	113	1824	SO[1509]	-11605.64	243
1723	SO[1408]	-10090.9	113	1774	SO[1459]	-10855.77	243	1825	SO[1510]	-11620.64	113
1724	SO[1409]	-10105.89	243	1775	SO[1460]	-10870.77	113	1826	SO[1511]	-11635.64	243
1725	SO[1410]	-10120.89	113	1776	SO[1461]	-10885.76	243	1827	SO[1512]	-11650.64	113
1726	SO[1411]	-10135.89	243	1777	SO[1462]	-10900.76	113	1828	SO[1513]	-11665.63	243
1727	SO[1412]	-10150.89	113	1778	SO[1463]	-10915.76	243	1829	SO[1514]	-11680.63	113
1728	SO[1413]	-10165.88	243	1779	SO[1464]	-10930.76	113	1830	SO[1515]	-11695.63	243
1729	SO[1414]	-10180.88	113	1780	SO[1465]	-10945.75	243	1831	SO[1516]	-11710.63	113
1730	SO[1415]	-10195.88	243	1781	SO[1466]	-10960.75	113	1832	SO[1517]	-11725.62	243
1731	SO[1416]	-10210.88	113	1782	SO[1467]	-10975.75	243	1833	SO[1518]	-11740.62	113
1732	SO[1417]	-10225.87	243	1783	SO[1468]	-10990.75	113	1834	SO[1519]	-11755.62	243
1733	SO[1418]	-10240.87	113	1784	SO[1469]	-11005.74	243	1835	SO[1520]	-11770.62	113
1734	SO[1419]	-10255.87	243	1785	SO[1470]	-11020.74	113	1836	SO[1521]	-11785.61	243

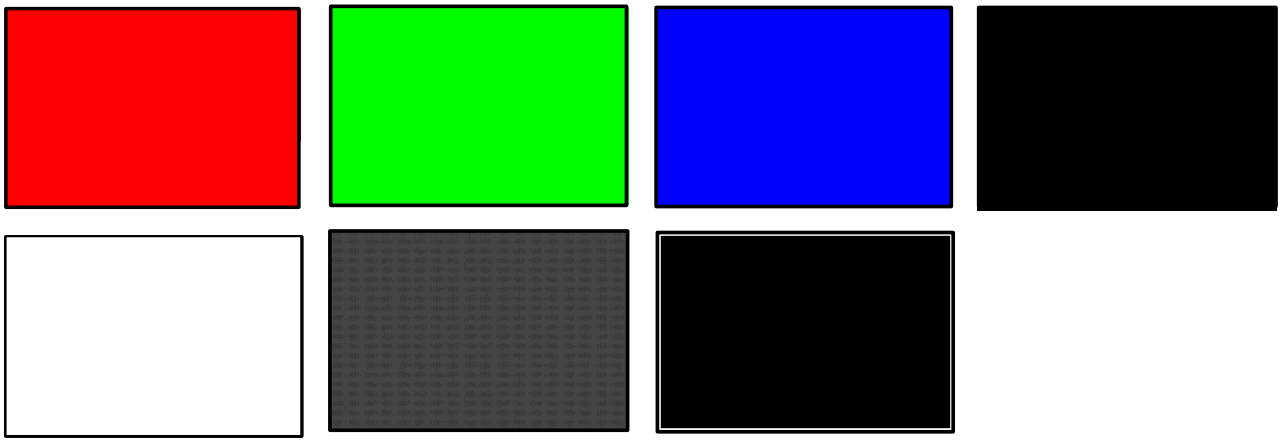
Pad	Name	X	Y	Pad	Name	X	Y	Pad	Name	X	Y
1837	SO[1522]	-11800.61	113								
1838	SO[1523]	-11815.61	243								
1839	SO[1524]	-11830.61	113								
1840	SO[1525]	-11845.6	243								
1841	SO[1526]	-11860.6	113								
1842	SO[1527]	-11875.6	243								
1843	SO[1528]	-11890.6	113								
1844	SO[1529]	-11905.59	243								
1845	SO[1530]	-11920.59	113								
1846	SO[1531]	-11935.59	243								
1847	SO[1532]	-11950.59	113								
1848	SO[1533]	-11965.58	243								
1849	SO[1534]	-11980.58	113								
1850	SO[1535]	-11995.58	243								
1851	SO[1536]	-12010.58	113								
1852	SHIELDING	-12053.04	258								
1853	COM1_OUT	-12103.04	258								
1854	COM1_OUT	-12153.04	258								
1855	SHIELDING	-12203.04	258								
1856	F_CTRLR	-12403	278								
1857	OEVR	-12303	238								
1858	SYNC1R	-12403	198								
1859	SYNC2R	-12303	158								
1860	UDR	-12403	118								
1861	CKVR	-12303	78								
1862	STV2R	-12403	38								
1863	STV1R	-12303	-2								
1864	F_CTRLR	-12403	-42								
1865	STBNR	-12303	-82								
	ALI_L	-12131.5	115.5								
	ALI_R	12131.5	115.5								

All pad location has considered thermal shifting. (After bonding)

Appendix A: BIST pattern

R→ G→ B→ Black→ White→Flicker pattern→Black background with white out Frame.

Note: Every Pattern stands 2 Seconds



Revision History

Version No.	Date	Page	Description
1.00	2019/02/21	All	New create